SiGe HBT Technology: A New Contender for Si-Based RF and Microwave Circuit Applications

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(Invited Paper)

***Abstract*—The silicon–germanium heterojunction bipolar transistor (SiGe HBT) is the first practical bandgap-engineered device to be realized in silicon. SiGe HBT technology combines transistor performance competitive with III–V technologies with the processing maturity, integration levels, yield, and hence, cost commonly associated with conventional Si fabrication. In the ten-and-one-half years since the first demonstration of a functional transistor, SiGe HBT technology has emerged from the research laboratory, entered manufacturing on 200-mm wafers, and is poised to enter the commercial RF and microwave market. State-of-the-art SiGe HBT's can deliver: 1) f_T in excess of 50 GHz; 2) $f_{\max}$ in excess of 70 GHz; 3) minimum noise figure below 0.7 dB at 2.0 GHz; 4) $1/f$ noise corner frequencies below 500 Hz; 5) cryogenic operation; 6) excellent radiation hardness; 7) competitive power amplifiers; and 8) reliability comparable to Si. A host of record-setting digital, analog, RF, and microwave circuits have been demonstrated in the past several years using SiGe HBT's, and recent work on passives and transmission lines on Si suggest a migratory path to Si-based monolithic microwave integrated circuits (MMIC's) is possible. The combination of SiGe HBT's with advanced Si CMOS to form an SiGe BiCMOS technology represents a unique opportunity for Si-based RF system-on-a-chip solutions. This paper reviews state-of-the-art SiGe HBT technology and assesses its potential for current and future RF and microwave systems.**

***Index Terms*—Bandgap engineering, BiCMOS, heterojunction bipolar transistor, microwave circuits, radio-frequency circuits, SiGe HBT, silicon–germanium.**

I. Bandgap Engineering in Silicon

WE LIVE in a silicon world. Greater than 95% of today's $200+ billion global semiconductor market uses the semiconductor silicon (Si) to realize a host of integrated circuits (IC's) ranging from 233-MHz microprocessors to 64-Mb dynamic random-access memory (DRAM) chips. Indeed, it is the very existence of Si microelectronics which has enabled the emergence of the Information Age which is so profoundly reshaping the way we live and work and play. Why Si? This profound market dominance of Si rests on a number of surprisingly practical advantages Si has over the other numerous semiconductors, including: 1) an extremely high-quality dielectric (SiO_2) can be trivially grown on Si and used for isolation, passivation, or as an active layer (e.g., gate oxide); 2) Si can be grown in very large, virtually defect-free single crystals (200 mm in production today, rapidly moving to 300 mm), yielding many (low-cost) IC's per wafer; 3) Si has excellent thermal properties allowing for the efficient removal of dissipated heat; 4) Si can be controllably doped with both n- and p-type impurities with extremely high dynamic range (10^{14}–10^{22} cm^{-3}); 5) Si has excellent mechanical strength, facilitating ease of handling and fabrication; 6) it is easy to make very low-resistance ohmic contacts to Si, thus minimizing device parasitics; and 7) Si is extremely abundant (think beach sand) and easily purified. Thus, from an IC manufacturing standpoint, Si is a dream come true.

Yet from a device designer's viewpoint, Si is hardly the ideal semiconductor. The carrier mobility (physically relating the velocity of the carriers to the applied electric field) for both electrons and holes in Si is rather small, and the maximum velocity that these carriers can attain is limited to about 1×10^7 cm/s under normal conditions. Since the speed of a device ultimately depends on how fast the carriers can be "pushed" through the device under practical operating voltages, Si can thus be regarded as a somewhat "slow" semiconductor. In addition, because Si is an indirect gap semiconductor, light emission is painfully inefficient, making optical devices such as lasers impractical. Many of the III–V compound semiconductors (e.g., GaAs or InP), on the other hand, enjoy far higher mobilities and saturation velocities and, because of their direct gap nature, make excellent optical devices. In addition, III–V devices, by virtue of the way they are grown, can be compositionally tailored for a specific need or application. This "bandgap engineering," as it is known, yields a large performance advantage for III–V technologies. Unfortunately, these benefits commonly associated with III–V semiconductors pale in comparison to the practical deficiencies associated with making highly integrated low-cost IC's from these materials. There is no decent grown oxide for GaAs or InP, for instance, and wafers are smaller with much higher defect densities, more prone to breakage, poorer heat conductors, etc. This translates into generally lower levels of integration, more difficult fabrication, lower yield, and ultimately higher cost. In truth, of course, III–V materials such as GaAs and InP fill important niche markets today (e.g., GaAs MESFET's for cell phones, AlGaAs- or InP-based lasers), but III–V

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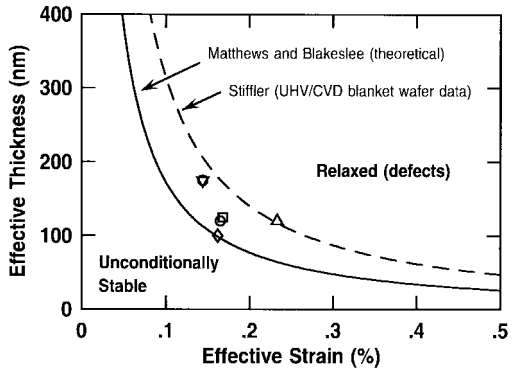

Fig. 1. Film-stability space showing effective thickness as a function of effective strain for SiGe films grown on Si.

semiconductor technologies will never become mainstream if Si-based technologies can "do the job."

While Si IC's are well-suited to low-cost high-volume microprocessors and memory applications, RF and microwave circuit applications, which by definition operate at much higher frequencies, generally place much more restrictive performance demands on the transistor building blocks. In this regime, the poorer intrinsic speed of Si devices becomes problematic. That is, even if Si IC's are cheap, they must deliver the required device performance to produce a competitive system at a given frequency. If not, then the higher priced, but faster, III–V technologies will dominate (as they indeed have to date in the RF and microwave markets).

The fundamental question then becomes simple and imminently practical: is it possible to improve the performance of Si transistors enough to be competitive with III–V devices for RF and microwave applications, while preserving the enormous yield, cost, and manufacturing advantages associated with conventional Si fabrication? As will be argued in this paper, the answer is "yes." This work reviews the achievements to date in using silicon–germanium (SiGe) alloys to practice bandgap engineering in the Si material system, and to thus achieve the stated goal.

While the idea of using SiGe alloys to bandgap-engineer Si devices dates to the 1960's, the synthesis of defect-free SiGe films proved quite difficult, and device-quality SiGe films were not successfully produced until the early to mid-1980's. While Si and Ge can be combined to produce a chemically stable alloy ($Si_{1-x}Ge_x$ or simply "SiGe"), their lattice constants differ by roughly 4% and, thus, SiGe alloys grown on Si substrates are compressively strained. (This is referred to as "pseudomorphic" growth of SiGe on Si, with the SiGe film adopting the underlying Si lattice constant.) These SiGe strained layers are subject to a fundamental stability criterion [1], [2], limiting their thickness for a given Ge concentration. Fig. 1 shows this stability diagram, which plots effective film thickness as a function of effective film strain (i.e., Ge content). Deposited SiGe films that lie below the stability curve are thermodynamically stable, and can be processed using conventional furnace or rapid-thermal annealing, ion-implantation, etc., without generating defects. Deposited SiGe films that lie above the stability curve, however, are "metastable" and will relax to their natural lattice constant if exposed to temperatures above the original growth temperature, generating device-killing defects in the process. For a manufacturable SiGe technology, it is obviously key that the SiGe films remain stable after processing. Shown in Fig. 1 are actual ultrahigh vacuum/chemical vapor deposition (UHV/CVD) SiGe films used in the devices presented in this paper, which are thermodynamically stable as grown with respect to the empirical stability curve for UHV/CVD films [3].

Introducing Ge into Si has a number of consequences. First and most importantly, because Ge has a larger lattice constant than Si, the energy bandgap of Ge is smaller than that of Si (0.66 eV versus 1.12 eV), and we thus expect SiGe to have a bandgap smaller than that of Si, making it a suitable candidate for bandgap engineering in Si. The compressive strain associated with SiGe alloys produces an additional bandgap shrinkage, and the net result is a bandgap reduction of approximately 7.5 meV for each 1% of Ge introduced. This Ge-induced "band offset" occurs predominantly in the valence band, making it conducive for use in n-p-n bipolar transistors. In addition, the compressive strain lifts the conduction and valence band degeneracies at the band extremes, effectively reducing the density of states and improving the carrier mobilities with respect to pure Si (the latter due to a reduction in carrier scattering). Because a practical SiGe film must be very thin if it is to remain stable and, hence, defect free, it is a natural candidate for use in the base region of a bipolar transistor (which, by definition, must be thin to achieve high-frequency performance). The resultant device contains an n-Si/p-SiGe emitter–base (EB) heterojunction and a p-SiGe/n-Si base–collector heterojunction and, thus, this device is properly called an "SiGe double-heterojunction bipolar transistor," although for clarity we will continue the standard usage of "SiGe heterojunction bipolar transistor" (SiGe HBT). The SiGe HBT represents the first practical bandgap-engineered Si-based transistor.

Technical progress in bringing SiGe HBT technology to reality has been exceptionally rapid. The first functional SiGe HBT was demonstrated in December 1987, only ten-and-one-half years ago [4], [5]. Worldwide attention was directed toward the technology in mid-1990 by the demonstration of a nonself-aligned SiGe HBT with a cutoff frequency (f_T) of 75 GHz [6]. At the time, this result was roughly twice the performance of state-of-the-art Si bipolar junction transistors (BJT's) (see Fig. 2), and clearly demonstrated the performance potential of the technology. Eyebrows were lifted. Later that same year, the first emitter-coupled logic (ECL) ring oscillators using self-aligned SiGe HBT's were produced [7]. The first SiGe BiCMOS technology was reported in 1992 [8], and the first large-scale integrated (LSI) circuit (a 1.2-GSample/s digital-to-analog converter) in 1993 [9]. The first SiGe HBT's with frequency response greater than 100 GHz were demonstrated in 1993–1994 [10]–[12], and the first SiGe HBT technology entered commercial production on 200-mm wafers in 1994 [13]. During this ten-and-one-half-year evolution, a large number of different SiGe HBT technologies have been demonstrated at laboratories throughout the world, using a variety of SiGe epitaxial growth techniques [14]–[31], and during

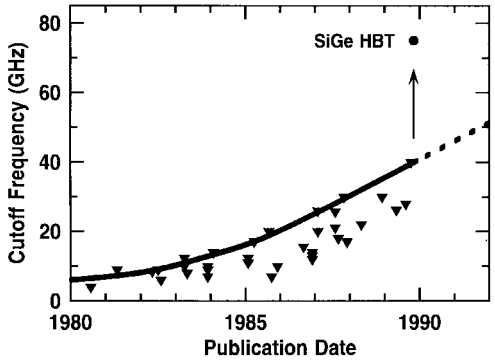

Fig. 2. Transistor cutoff frequency as a function of publication date showing the first high-frequency SiGe HBT result.

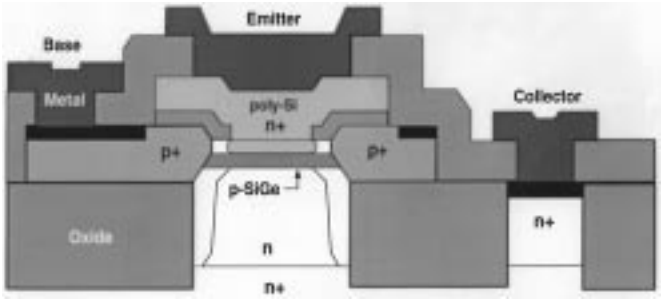

Fig. 3. Schematic device cross section of a self-aligned SiGe HBT.

TABLE I
ELEMENTS IN IBM's SiGe BiCMOS TECHNOLOGY [28]

Element	Characteristics
Standard SiGe HBT	47 GHz f_T at $BV_{\mathrm{CEO}} = 3.3$ V
High-Breakdown SiGe HBT	28 GHz f_T at $BV_{\mathrm{CEO}} = 5.3$ V
Si CMOS	0.36 μm L_{eff} for 2.5 V V_{DD}
Gated Lateral p-n-p	1.0 GHz f_T
Polysilicon Resistor	342 $\Omega/\square$
Ion-Implanted Resistor	1600 $\Omega/\square$
Thin-Oxide Decoupling Capacitor	1.5 fF/μm^2
MIM Precision Capacitor	0.70 fF/μm^2
Inductor (6-turn)	10 nH with $Q = 10$ at 1.0 GHz
Schotty Barrier Diode	213 mV at 100 μA
p-i-n Diode	790 mV at 100 μA
Varactor Diode	810 mV at 100 μA
ESD Diode	1.2 kV

the past two to three years, these technologies have produced a large number of impressive circuit demonstrations for practical digital, RF, and microwave applications [32]–[51]. Robust and manufacturable SiGe HBT technologies potentially suitable for commercial applications now exist in the U.S., Europe, and Japan [13], [19], [21]–[23], [26], [27], [30]. Various review papers dealing with SiGe materials, devices, and technologies can be found in [52]–[60].

This review paper takes a somewhat different approach and will examine the potential of SiGe HBT technology explicitly for RF and microwave circuit applications. As with any viable RF or microwave system, the transistor by itself is only one component of the final product. For this reason, technology issues associated with passive elements, transmission lines, and manufacturability are also addressed. Testing and packaging issues, though obviously very important in this context, will not be discussed due to space constraints. This paper is organized in the following manner. Section II introduces the reader to state-of-the-art SiGe HBT technology. Section III addresses the transistor-level dc and ac device physics and performance capabilities of state-of-the-art SiGe HBT's. Section IV turns to the technology-related issues associated with using SiGe HBT's for practical RF and microwave circuit applications. Finally, Section V reviews the state-of-the-art device and circuit performance and addresses the fundamental performance limits of SiGe HBT technology.

II. SiGe HBT TECHNOLOGY

In order to provide a logical framework for this paper, the experimental results presented will be largely from IBM's SiGe HBT technology [25]. This technology is representative of the state-of-the-art in 1998, is currently qualified and in commercial production on 200-mm wafers in an advanced CMOS fabrication facility, and is thus arguably the most "real" SiGe HBT technology worldwide. The basic tenets which dictate the final implementation of IBM's SiGe HBT technology are: 1) maintain strict processing compatibility with existing CMOS tool sets and metallization schemes; 2) use only thermodynamically stable SiGe films that can be deposited using a batch process in manufacturing mode on large (200-mm) wafers; 3) choose an SiGe HBT device structure which naturally preserves a path to SiGe BiCMOS integration without compromising the SiGe HBT performance; and 4) provide an additional suite of passive and active technology elements required for realizing monolithic RF and microwave functions. There are, in fact, a number of other viable SiGe HBT technologies currently in existence with at least potentially comparable transistor-level performance [19], [21]–[23], [26], [27], [30]. While the tenets shaping these competing technologies are not necessarily coincident with those listed above, the results and conclusions presented in this paper are sufficiently general that they can be easily extended to all SiGe HBT technologies in a reasonably straightforward manner.

Fig. 3 shows a schematic device cross section of the SiGe HBT (for clarity, the deep-trench isolation and multilevel metallization are not shown in this view). This SiGe HBT has a planar self-aligned structure with a conventional polysilicon emitter contact, silicided extrinsic base, and deep- and shallow-trench isolation. A three-to-five-level chemical–mechanical-polishing (CMP) planarized W-stud AlCu CMOS metallization scheme is used. The extrinsic resistive and capacitive parasitics are intentionally minimized to improve the maximum oscillation frequency $(f_{\max})$ of the transistor, and the minimum device geometry has an emitter area of 0.5×1.0 μm^2. The fabrication steps used to produce this SiGe HBT are covered in detail elsewhere [59]. This SiGe HBT has been successfully integrated with conventional high-performance Si CMOS to realize a SiGe BiCMOS technology [28]. The SiGe HBT dc and ac characteristics in the SiGe BiCMOS technology are essentially identical with the standalone SiGe HBT technology, and will only be explicitly distinguished in this paper when appropriate. Table I shows the suite of

TABLE II
TYPICAL PARAMETERS FOR AN SiGe HBT WITH $A_E = 0.5 \times 2.5\ \mu\text{m}^2$ [28]. ALL AC PARAMETERS WERE MEASURED AT $V_{CB} = 1.0$ V AND $f_{\max}$ WAS EXTRACTED USING MAXIMUM AVAILABLE GAIN (MAG)

Parameter	Standard SiGe HBT	High-BV_{CEO} SiGe HBT
peak β	113	97
V_A (V)	61	132
βV_A (V)	6893	12 804
peak f_T (GHz)	48	28
r_{bb} at peak f_T (Ω)	80	N/A
peak $f_{\max}$ (GHz)	69	57
BV_{CEO} (V)	3.3	5.3
BV_{EBO} (V)	4.2	4.1
peak $f_T \times BV_{\text{CEO}}$ (GHz V)	158	143

TABLE III
TYPICAL PARAMETERS FOR A W/L = 20.0 μm/0.5μm (drawn) n-FET AND p-FET FROM THE SiGe BiCMOS TECHNOLOGY DESCRIBED IN TABLE I [28]

Parameter	n-FET	p-FET
gate material	n^+ poly	p^+ poly
L_{eff} (μm)	0.36	0.36
t_{ox} (nm)	7.8	7.8
V_{DD} (V)	3.3	3.3
V_T (V)	0.58	−0.55
$g_{m,\text{sat}}$ (mS/mm)	190	103
$R_{\text{S/D}}$ ($\Omega\mu$m)	440	2000
$I_{D,\text{sat}}$ (μm)	468	231

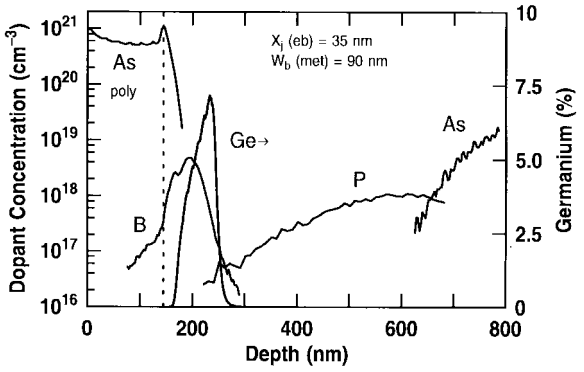

Fig. 4. Typical secondary ion mass spectroscopy (SIMS) doping profile of an SiGe HBT.

resultant elements in this SiGe BiCMOS technology. Two SiGe HBT's are available, one with a reduced collector implant and, hence, higher BV_{CEO} (5.3 V versus 3.3 V) that is suitable for RF power applications. Tables II and III give the typical SiGe HBT and Si CMOS device parameters at 300 K [28].

A representative doping profile of an advanced SiGe HBT is shown in Fig. 4. The *in-situ* boron-doped graded SiGe base is deposited across the entire wafer using the UHV/CVD technique [61]. In areas that are not covered by oxide, the UHV/CVD film consisting of an intrinsic-Si/strained boron-doped SiGe/intrinsic-Si stack is deposited as a perfect single-crystal layer on the Si substrate. Over the oxide, the deposited layer is polycrystalline (poly), and will serve either as the extrinsic base contact of the SiGe HBT, the poly-on-oxide resistor, or the gate electrode of the Si CMOS devices. Observe that the Ge profile is graded across the neutral base. The peak

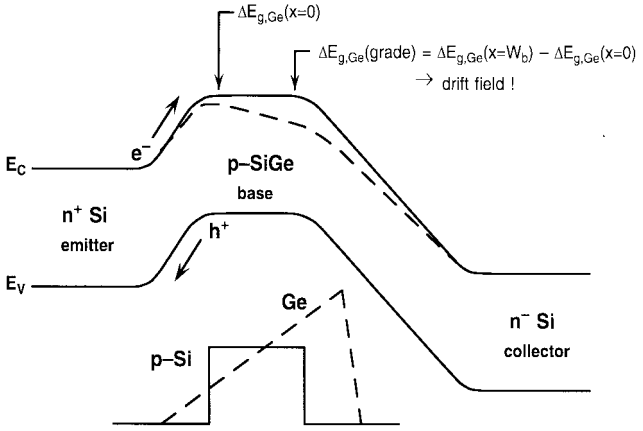

Fig. 5. Energy band diagram of a graded-base SiGe HBT compared to an Si BJT.

Ge content in typical profiles ranges from 8% to 15% and are thermodynamically stable as grown. The metallurgical base and single-crystal emitter widths range from 75 to 90 nm and 25 to 35 nm, respectively. A masked phosphorus implant is used to tailor the intrinsic collector profile for optimum frequency response at high current densities.

Because of its compatibility with Si CMOS fabrication, with its inherently significant thermal cycle, the resultant *emitter/base/collector* doping profile of such an SiGe HBT looks far more like that of a conventional ion-implanted base Si BJT (with a heavily doped poly emitter and moderately doped base) than a conventional III–V HBT (with a lightly doped emitter and very thin and heavily doped base). SiGe HBT's with doping profiles more closely resembling conventional III–V HBT's have been demonstrated [17], but by definition they are typically zero-thermal cycle ("0-Dt") mesa-isolated structures with metastable SiGe profiles and, hence, are not compatible with CMOS fabrication, high levels of integration, and low-cost manufacturing. For this reason, they will not be addressed in detail here. We turn next to the basic dc and ac operational characteristics of this device.

III. THE SiGe HBT

This section gives an overview of the performance capabilities of state-of-the-art SiGe HBT's. Basic device physics, dc and ac performance advantages over Si BJT's, low-frequency and broad-band noise characteristics, radiation tolerance, temperature effects, and reliability issues are addressed. For brevity, only the final results of the basic device physics derivations are included. The interested reader is referred to [58] for more complete derivations.

A. DC Characteristics

The dc consequences of introducing Ge into the base region of an SiGe HBT can best be understood by considering an energy-band diagram of the resultant device and comparing it to Si. As shown in Fig. 5 by the dashed line, the Ge is compositionally graded from low concentration at the EB junction to high concentration at the collector–base (CB) junction. The impact on the SiGe HBT band diagram is also

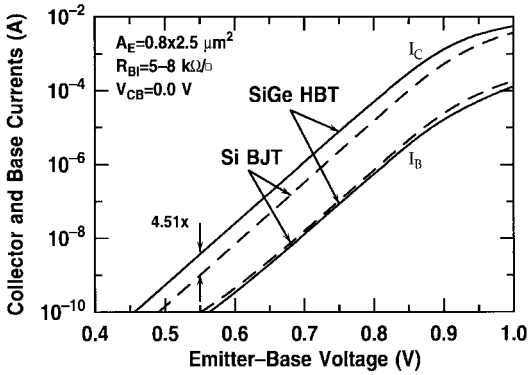

Fig. 6. Comparison of the collector and base currents as a function of EB voltage for an SiGe HBT and an Si BJT of comparable doping profile.

shown and consists of a finite band offset at the EB junction $[\Delta E_{g,\mathrm{Ge}}(x=0)]$ as well as a larger band offset at the CB junction $[\Delta E_{g,\mathrm{Ge}}(x=W_b)]$. The position dependence of the band offset with respect to Si is conveniently expressed as a bandgap grading term $[\Delta E_{g,\mathrm{Ge}}\ (\mathrm{grade}) = \Delta E_{g,\mathrm{Ge}}(W_b) - \Delta E_{g,\mathrm{Ge}}(0)]$. Physically this position dependence in the Ge-induced band offset produces an electric field in the neutral base region which aids the transport of minority carriers (electrons) from emitter to collector, thereby improving frequency response.

The important dc consequence of adding Ge into the base, however, lies with the collector current density (J_C). Physically, the barrier to electron injection at the EB junction is reduced by introducing Ge into the base, yielding more charge transport from emitter-to-collector for a given applied EB bias. Observe from Fig. 5 that in this graded-base design, the emitter region of the SiGe HBT and Si BJT comparison are essentially identical, implying that the resultant base current density (J_B) of the two transistors will be roughly the same. The net result is that the introduction of Ge increases the current gain of the transistor $(\beta = J_C/J_B)$. From a more device–physics-oriented viewpoint, the Ge-induced band offset exponentially decreases the intrinsic carrier density in the base which, in turn, decreases the base Gummel number and, hence, increases J_C. Meaningful in this context is the Ge-induced improvement in β over a comparably constructed Si BJT

$$\frac{J_{C,\mathrm{SiGe}}}{J_{C,\mathrm{Si}}} = \frac{\beta_{\mathrm{SiGe}}}{\beta_{\mathrm{Si}}} = \gamma\eta \frac{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT e^{\Delta E_{g,\mathrm{Ge}}(0)/kT}}{1 - e^{-\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}} \tag{1}$$

where $\gamma = N_C N_V(\mathrm{SiGe})/N_C N_V(\mathrm{Si})$ is the ratio of the density-of-states product between SiGe and Si, and $\eta = D_{\mathrm{nb}}(\mathrm{SiGe})/D_{\mathrm{nb}}(\mathrm{Si})$ accounts for the differences between the electron and hole mobilities in the base. As can be seen in Fig. 6, which compares the measured Gummel characteristics for two identically-constructed SiGe HBT's and Si BJT's, these theoretical expectations are clearly borne out in practice.

The exponential dependence of β in an SiGe HBT on the EB boundary value of the Ge-induced band offset provides a powerful lever for tailoring β for a specific need and, importantly, effectively decouples β from the specifics of the base doping profile. For instance, in applications which do not require large values of β, the base can be more heavily doped to reduce the base resistance (R_b) without a negative impact on β, as would be the case in an Si BJT. That is, we can trade β for lower R_b to yield enhanced frequency response and better broad-band noise performance. This Ge lever can also be used to engineer an SiGe HBT whose β is independent of temperature [58], a decided advantage over Si BJT's from a circuit standpoint.

Another dc benefit to using a graded Ge profile is an exponential enhancement in output conductance [reflected in the Early voltage (V_A)]. Compared to an Si BJT of identical doping, V_A is enhanced according to

$$\frac{V_{A,\mathrm{SiGe}}}{V_{A,\mathrm{Si}}} = e^{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}\left[\frac{1 - e^{-\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}}{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}\right]. \tag{2}$$

Physically, the Ge grading "weights" the base profile toward the CB side of the neutral base, making it effectively harder to deplete for a given bias than a identically constructed Si BJT. The V_A for the SiGe HBT and Si BJT (shown in Fig. 6) are 53 V versus 18 V, respectively. An important figure of merit for analog applications such as high-speed data converters and precision current sources is the so-called "current gain–Early voltage product" (βV_A product). For an SiGe HBT, the βV_A product is strongly enhanced over a comparably designed Si BJT according to

$$\frac{\beta V_A|_{\mathrm{SiGe}}}{\beta V_A|_{\mathrm{Si}}} = \gamma\eta e^{\Delta E_{g,\mathrm{Ge}}(0)/kT} e^{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}. \tag{3}$$

Since the βV_A product in an SiGe HBT depends exponentially on both the EB band offset and the Ge grading, it can thus be made almost arbitrarily large in applications which require it.

B. Frequency Response

In most RF and microwave circuit applications, it is the transistor frequency response that limits system performance. An important figure of merit in bipolar transistors is the unity–gain cutoff frequency (f_T), which is given by

$$f_T = \left[\frac{1}{g_m}(C_{\mathrm{eb}} + C_{\mathrm{cb}}) + \tau_b + \tau_e + \tau_c\right]^{-1} \tag{4}$$

where g_m is the transconductance, C_{eb} and C_{cb} are the EB and CB capacitances, and τ_b, τ_e, τ_c are the base, emitter, and collector transit times, respectively. The f_T of a transistor in principle samples only the vertical profile, and is thus a useful metric for comparing various technologies. In conventional Si BJT's, τ_b typically limits the maximum f_T of the transistor. The built-in electric field induced by the Ge grading across the neutral base effectively decreases τ_b since, physically, the carriers are more rapidly accelerated across the base. With respect to an identically constructed Si BJT we find

$$\frac{\tau_{b,\mathrm{SiGe}}}{\tau_{b,\mathrm{Si}}} = \frac{2}{\eta}\left(\frac{kT}{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})}\right) \times \left[1 - \frac{1 - e^{-\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}}{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}\right]. \tag{5}$$

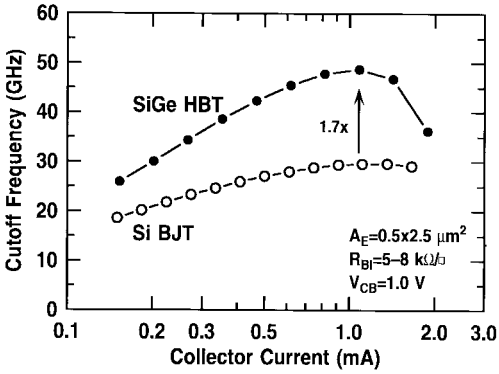

Fig. 7. Comparison of the cutoff frequency as a function of bias current for an SiGe HBT and an Si BJT of comparable doping profile.

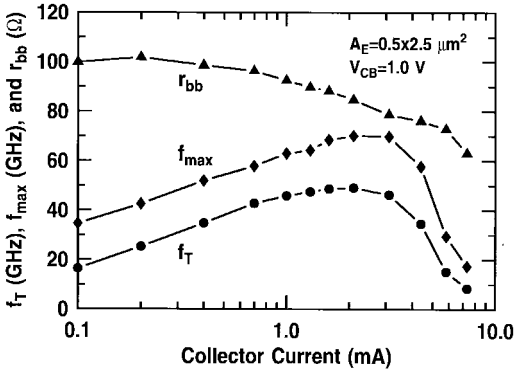

Fig. 8. Transistor cutoff frequency, base resistance, and maximum oscillation frequency as a function of bias current for a 0.5 × 2.5 μm^2 commercial UHV/CVD SiGe HBT.

In addition, since τ_e is reciprocally related to the ac β of the transistor, the band offset at the EB junction also serves to improve the SiGe HBT frequency response since

$$\frac{\tau_{e,\mathrm{Si}}}{\tau_{e,\mathrm{SiGe}}} = \frac{\beta_{\mathrm{SiGe}}}{\beta_{\mathrm{Si}}} = \gamma\eta \frac{\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT e^{\Delta E_{g,\mathrm{Ge}}(0)/kT}}{1 - e^{-\Delta E_{g,\mathrm{Ge}}(\mathrm{grade})/kT}}. \tag{6}$$

While τ_e is not typically a limiting transit time in state-of-the-art polysilicon-emitter devices, it will become increasingly important as the vertical profile is scaled to thinner dimensions with further technology evolution. The net result is that the peak f_T of an SiGe HBT will improve significantly over a comparably designed Si BJT, as is shown experimentally in Fig. 7, where the improvement is about 1.7×. Observe that in Fig. 7 the frequency response of the SiGe HBT is significantly higher than for the Si BJT over a wide range of operating bias (they do, in fact, converge at sufficiently low bias currents). The potential thus exists to operate the SiGe HBT at a frequency lower than the peak f_T, but at a significantly reduced bias current to realize a significant power savings. This frequency-power dissipation tradeoff is a potentially important one for portable system applications, which frequently have stringent power consumption constraints. In Fig. 7, for instance, if a given circuit application requires an f_T of only 30 GHz, the bias current for the SiGe HBT can be dropped by almost 6× compared to the Si BJT.

The unity power-gain frequency, or maximum oscillation frequency $(f_{\max})$, is a more relevant figure of merit for practical RF and microwave applications since it depends not only on the intrinsic transistor performance (f_T), but also the parasitics of the device, according to

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_{\mathrm{cb}} r_{\mathrm{bb}}}} \tag{7}$$

where C_{cb} is the total CB capacitance and r_{bb} is the total ac base resistance. Fig. 8 shows the bias dependence of f_T, $f_{\max}$, and r_{bb} for a 0.5 × 2.5 μm^2 transistor from the state-of-the-art SiGe HBT BiCMOS technology [28]. The $f_{\max}$ of the transistor peaks at 65–70 GHz, competitive with current-generation III–V devices, with a total base resistance of less than 80 Ω at peak $f_{\max}$. Given that $f_{\max}$ is better correlated to actual circuit performance, it is not surprising that the enhanced $f_{\max}$ of SiGe HBT's over Si BJT's yields an improvement in ECL switching delay, as evidenced by the unloaded ring oscillator results shown in Fig. 9. A number of impressive ECL circuit results have been published in recent years using SiGe HBT's [7], [13], [15], [16], [21]–[23], [27], [31], [34].

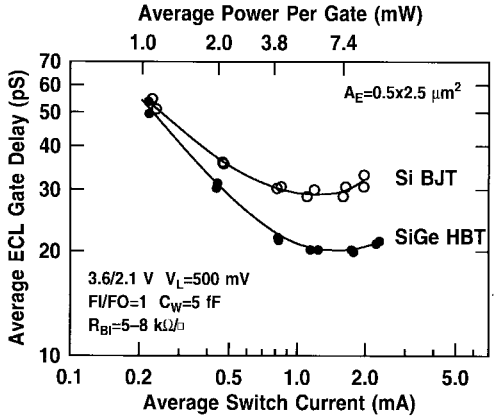

Fig. 9. Comparison of the gate delay of an unloaded ECL ring oscillator as a function of bias current for an SiGe HBT and an Si BJT of comparable doping profile.

C. Low-Frequency and Broad-Band Noise

Transistor noise performance, which can be virtually ignored in digital systems, becomes an important issue in RF and microwave communications system design. Transistor high-frequency (broad-band) noise plays a major role in system sensitivity since it sets the signal-to-noise level on the low-noise amplifier (LNA) at the input of the system. In addition, low-frequency $(1/f)$ noise places a fundamental limit on the spectral purity of the system because it up-converts to phase noise in the requisite mixers and oscillators in the system. Minimizing transistor broad-band and $1/f$ noise are thus key concerns in RF and microwave system design.

Because they are vertical transport bulk devices, high-speed Si BJT's are well known for their excellent $1/f$ noise performance [62], far lower than what can be realized in either Si CMOS, GaAs MESFET, GaAs high electron-mobility

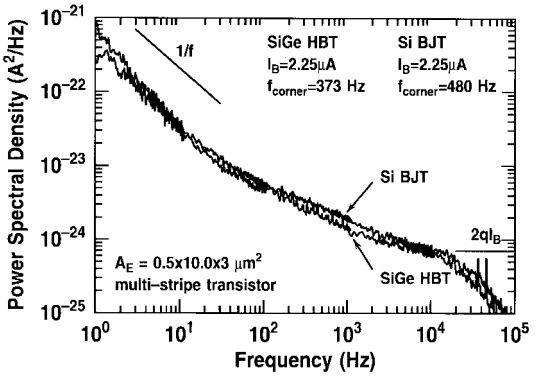

Fig. 10. Comparison of the low-frequency noise characteristics of an SiGe HBT and an Si BJT of comparable doping profile.

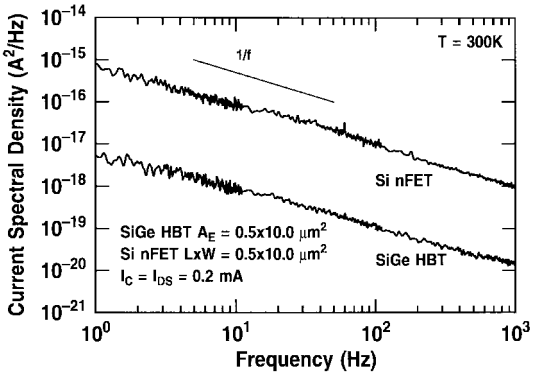

Fig. 12. Comparison of the low-frequency noise characteristics of an SiGe HBT and a conventional Si n-FET of identical geometry and bias.

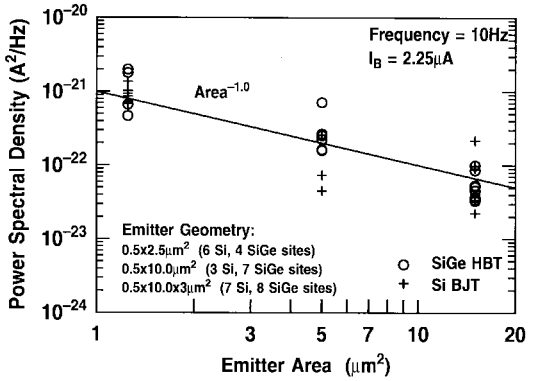

Fig. 11. Power spectral density at 10 Hz as a function of emitter area for comparably designed SiGe HBT's and Si BJT's.

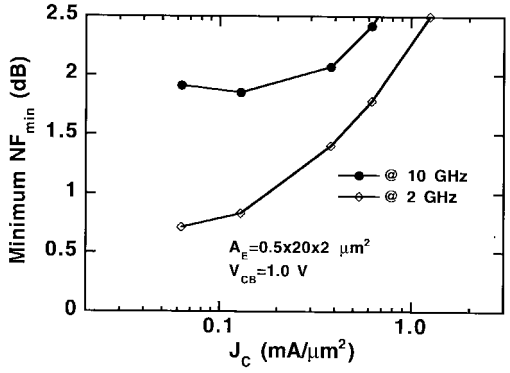

Fig. 13. Measured minimum noise figure as a function of current density at 2.0 and 10.0 GHz.

transistor (HEMT), or GaAs HBT technologies. It is thus very important that SiGe HBT's exhibit $1/f$ noise performance comparable to that obtainable in Si BJT's. As can be seen in Fig. 10, this is indeed the case [63]–[65]. The SiGe HBT shown in Fig. 10 achieves a sub-500 Hz $1/f$ noise corner frequency, comparable to the best Si BJT technologies, and far superior to that obtained in III–V HBT or FET technologies [66], [67]. Fig. 11 shows statistical measurements of the power spectral density at 10 Hz for a number of SiGe HBT's and Si BJT's of differing geometry. The fact that the $1/f$ noise magnitude is comparable between the SiGe HBT's and Si BJT's of identical area is significant since it suggests that there is no penalty paid in $1/f$ noise performance by using SiGe strained layers in the base region of the device. In addition, the noise magnitude decreases with increasing transistor size, a fact that is commonly exploited in noise-sensitive applications. The combination of an observed I_B^2 bias dependence and the $1/A_E$ geometry dependence can be used to infer the physical location of the traps participating in the noise processes [68]. In this case, the noise appears to be distributed uniformly across the emitter area of the device and are most likely associated with the polysilicon emitter contact [69]. It is interesting to compare the magnitude of the $1/f$ noise between a current-generation Si CMOS transistor and an SiGe HBT of identical geometry and operated at the same bias current. As can be seen in Fig. 12, the SiGe HBT enjoys nearly two orders of magnitude improvement in $1/f$ noise, and even a larger margin over GaAs MESFET's. This result will provide a key design advantage for SiGe HBT's in mixer and oscillator applications.

If the excellent $1/f$ noise properties of SiGe HBT's can be combined with excellent broad-band noise performance, then the technology would be uniquely suited for use in all transceiver building blocks, leading the way to more aggressive integration of transceiver functions, and presumably lower system cost. From basic noise theory, one clearly wants to minimize r_{bb}, increase f_T, and increase β to improve broad-band noise performance. Given that bandgap engineering is an ideal tool for accomplishing this, one might intuitively expect SiGe HBT's to be capable of excellent broad-band noise performance. This is indeed the case. Fig. 13 shows measured minimum noise figure ($\mathrm{NF_{min}}$) at both 2.0 and 10.0 GHz as a function of current density for a $0.5 \times 20 \times 2$ μm^2 multistripe transistor that might be used, for instance, in an LNA. These $\mathrm{NF_{min}}$ results, while not as low as what can be obtained in state-of-the-art III–V HEMT devices, are competitive with current-generation GaAs MESFET's and, importantly, can be obtained simultaneously with low $1/f$ noise. Even more aggressive $\mathrm{NF_{min}}$ results have been obtained in MBE-grown mesa-isolated SiGe HBT's [70].

Profile optimization to achieve even lower $\mathrm{NF_{min}}$ in the present SiGe HBT technology appears feasible. Fig. 14 shows the simulated noise factor at 10 GHz as a function of collector current density. In the present-generation SiGe HBT the collector partition noise dominates, not the base thermal

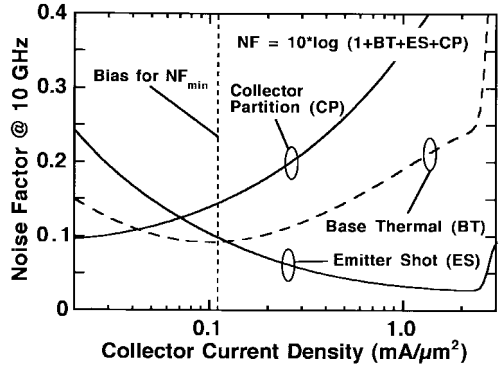

Fig. 14. Simulated noise factor as a function of collector current density showing the various components of broad-band noise in an SiGe HBT.

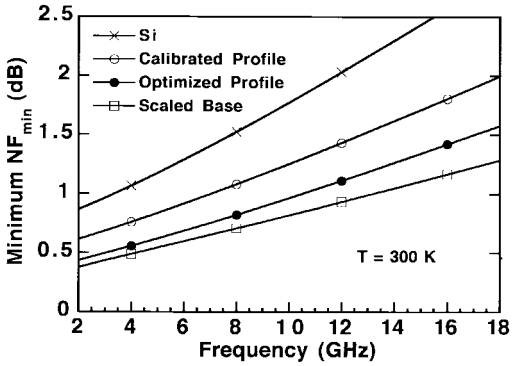

Fig. 15. Simulated minimum noise figure as a function of frequency for a Si BJT and SiGe HBT's with differing vertical profiles.

noise, as might be naively anticipated. Observe as well that the lowest value of $\mathrm{NF_{min}}$ occurs at a current density of only 0.1 mA/μm^2, over an order of magnitude below the current density at which $f_{\max}$ peaks, suggesting that very low-power, very low-noise LNA's should be feasible in SiGe HBT technology [45]. This also suggests that alternative doping and Ge profiles designed explicitly for optimizing broad-band noise performance should be possible [71]. Fig. 15 shows simulation results for minimum $\mathrm{NF_{min}}$ as a function frequency for a number of Ge profiles, one of which is calibrated to measured results. Observe that: 1) SiGe provides significant leverage over Si; 2) Ge profile optimization can provide further improvements; and 3) additional base profile scaling will be beneficial. Sub-0.5 dB $\mathrm{NF_{min}}$ at 2.0 GHz, sub-1.0 dB $\mathrm{NF_{min}}$ at 10 GHz, and sub-2.0 dB $\mathrm{NF_{min}}$ at 20 GHz appear to be reasonable goals for optimized SiGe HBT technology.

D. Radiation Tolerance

An important emerging market for RF and microwave circuit technologies is in space-born satellite systems, key components in the requisite infrastructure to support global communications networks for voice, video, and data transmission. Space is an amazingly hostile environment, due not only to the extreme temperature variations encountered between solar shade and solar illumination, but importantly from a radiation standpoint. The temperature extremes can be dealt with when needed by adding (costly) heating and

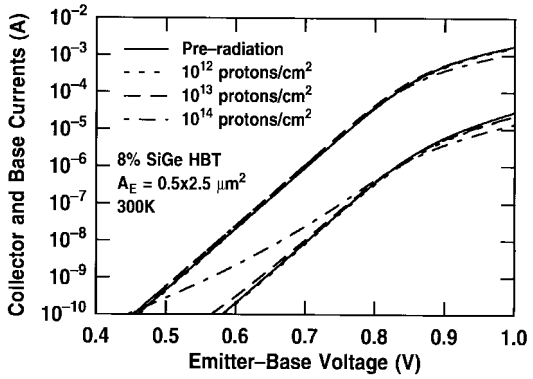

Fig. 16. Collector and base currents as a function of EB voltage showing the effects of proton irradiation on SiGe HBT's.

cooling systems, but the impact of radiation is much more severe since effective shielding of sensitive electronics from high-energy particles is impractical (it is hard to launch a satellite with two feet of lead shielding!). Depending on the orbital position and altitude, satellites are routinely exposed to large and potentially lethal fluxes of high-energy protons, neutrons, electrons, gamma rays (high-energy photons), x-rays, and cosmic rays (high-energy heavy ions). It is not uncommon for a satellite to be exposed to 10^{10}–10^{12} cm^{-2} of protons and 10–1000 krad (Si) of gamma dose over their flight lifetimes. Given the cost of building and launching a satellite, radiation-induced failures are highly unwelcome. For this reason, space-born electronics are subjected to exhaustive radiation testing, and usually require very costly "radiation-hardening" process, layout, and circuit-design modifications before they can be flown in space.

The "holy grail" in this context is to have a standard (terrestrial) device technology which is inherently radiation-hard as fabricated and, hence, space-qualified without any process or design modification. Preliminary results suggest that this is the case for SiGe HBT technology with respect to gamma rays [72], [73], neutrons [74], and protons [75]. Fig. 16 shows the Gummel characteristics of an SiGe HBT (which has not been radiation hardened in any way) both before and after exposure to 46-MeV protons at fluences ranging from 10^{12} to 10^{14} cm^{-2} (10^{14} cm^{-2} is a higher fluence than will be encountered in practical space orbits). For proton fluences up to 10^{13} cm^{-2} only minor shifts in the base current are observed, and negligible degradation in frequency response occurs [75]. Fig. 17 compares the impact of extreme radiation exposure of protons, neutrons, and gamma rays on the β of SiGe HBT's. As expected, proton irradiation has the most serious impact on device operation, since it produces both displacement damage as well as ionization damage. The observed degradation in β for all three radiation types is much smaller than that found in conventional Si BJT's (even radiation-hardened versions), as well as other SiGe HBT technologies [76], indicating that this SiGe HBT technology is inherently radiation hard. Experiments addressing the immunity of SiGe HBT circuits to cosmic-ray induced single-event effects (SEE's) and low-dose-rate gamma exposure are planned for the near future to complete the picture.

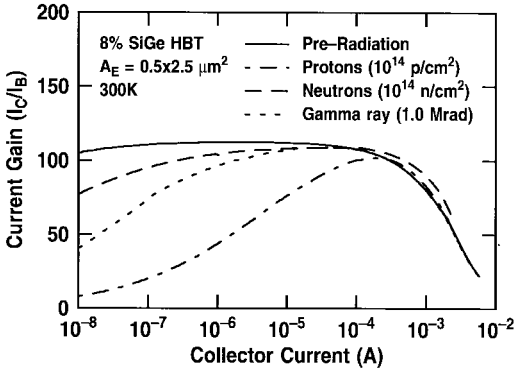

Fig. 17. Current gain as a function of collector current for an SiGe HBT both before and after exposure to: (a) 46 MeV, 1×10^{14} cm^{-2} proton fluence, (b) 1 MeV, 1×10^{14} cm^{-2} neutron fluence, and (c) 1.0 Mrad (Si) gamma radiation.

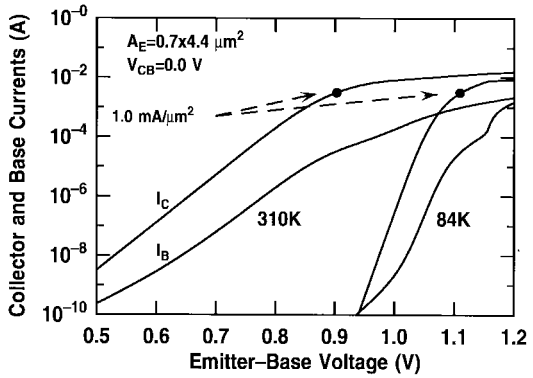

Fig. 18. Collector and base currents as a function of EB voltage at 310 and 84 K for an SiGe HBT.

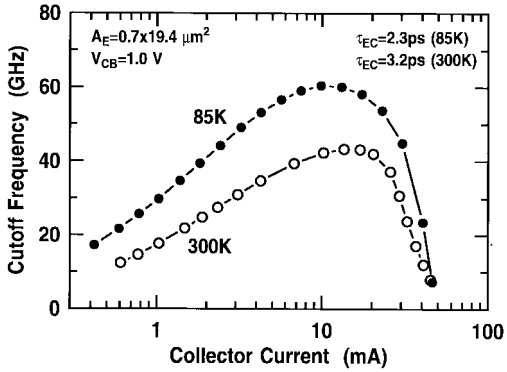

Fig. 19. Cutoff frequency as a function of bias current at 300 and 85 K for an SiGe HBT.

Comparison of the radiation tolerance of these SiGe HBT's to epi-base Si BJT's from the same fabrication run suggest that the SiGe *per se* is not the origin of the inherent radiation hardness of this technology, but rather is the result of the device structure itself. From a radiation immunity viewpoint, this SiGe HBT structure has several intrinsic advantages: 1) the EB spacer is very thin and composed of a radiation-hard oxide-nitride composite; 2) the extrinsic base doping under the EB spacer is very high, effectively confining any ionization damage in that region; 3) the active device region is very thin (<200 nm) and, hence, the total volume exposed to particle displacement damage is minimal; and 4) the deep- and shallow-trench isolation minimizes the exposure of oxides that can contribute to junction leakage. Preliminary radiation experiments using the Si CMOS devices in the full SiGe BiCMOS technology suggest that while the Si n-FET's are significantly less tolerant to ionizing radiation (gamma) than either the Si p-FET or the SiGe HBT, they are still as good as conventional radiation-hardened Si CMOS (with a dose tolerance of at least 50 krad). Thus, SiGe technology offers promise as a high-speed low-cost alternative for applications requiring some level of radiation tolerance.

E. Temperature Effects

Bandgap engineering generally has a very positive influence on the temperature characteristics of SiGe HBT's and thus allows the SiGe HBT to operate well in the cryogenic environment (e.g., liquid-nitrogen temperature = 77 K), a regime which is traditionally forbidden to Si BJT's [77]–[81]. At present, cryogenic electronics represents a small, but important niche market, with applications such as high-sensitivity cooled sensors and detectors, superconductor hybrid systems, space-born electronics, and further down the road, low-temperature computers. A cursory examination of (1)–(6) shows that both the dc and ac properties of SiGe HBT's should be favorably affected by cooling. This is indeed the case. Figs. 18 and 19 show the Gummel characteristics and frequency response of an SiGe HBT which has been explicitly optimized for 77-K operation [81]. At 84 K, this SiGe HBT has an output current drive greater than 1.0 mA/μm^2, a peak β of 500, a peak f_T of 60 GHz, and a peak $f_{\max}$ of 50 GHz, all significantly higher than their 300-K values. These advantages carry over to the circuit domain, yielding a record 22-ps ECL gate delay at 84 K, the first Si-based bipolar circuit to achieve faster speed at 84 K than at 300 K. While the large power dissipation associated with conventional bipolar digital circuit families such as ECL would preclude their widespread use in cooling-constrained cryogenic systems, the combination of cooled low-power Si CMOS with SiGe HBT's offering excellent frequency response, low-noise performance, radiation hardness, and excellent analog properties represents a unique opportunity for the use of SiGe BiCMOS technology in cryogenic systems.

Independent of potential cryogenic applications that may exist for SiGe BiCMOS technology, all electronic systems must operate well over an extended temperature range (e.g., −55 °C–125 °C for military specifications). Having the ability to controllably vary the Ge profile shape can serve as a powerful lever for the device designer in this context, since Ge-induced changes in the bandgap couple strongly to temperature in the device equations [refer to (1)–(6)]. For example, the proper choice for the Ge profile shape can yield an SiGe HBT which has a β with a zero temperature coefficient [58], a decided advantage for many circuit applications. There is a down side, of course. Unintentional and sometimes unavoidable effects associated with the presence of Ge-induced band offsets in the device can be troublesome. For instance, unique phenomena such as parasitic energy barriers due to

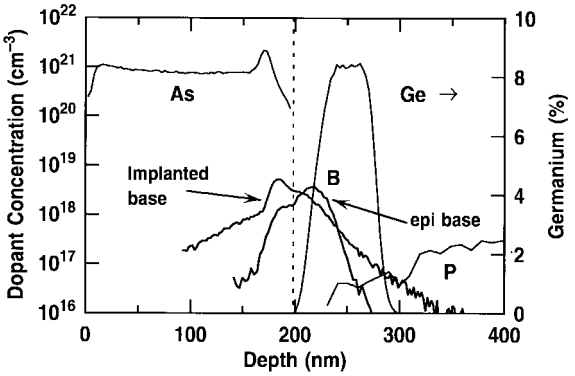

Fig. 20. Comparison of the base profiles of an aggressive ion-implanted Si BJT and an SiGe HBT.

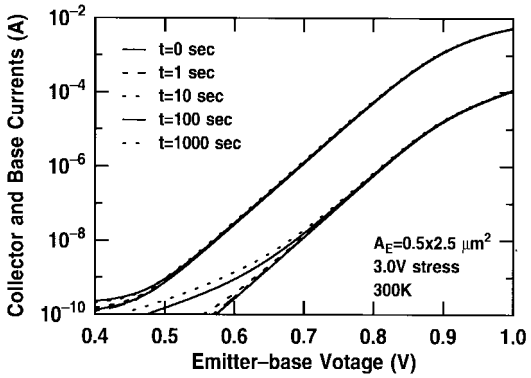

Fig. 21. Collector and base current as a function of EB voltage showing the effects of reverse-bias EB stress on an SiGe HBT.

Ge misplacement [82], Ge-ramp effect [83], [84], neutral base recombination [85], [86], and high-injection barrier effects [87] all have a strong temperature dependence and can negatively impact device performance. Careful profile optimization can generally alleviate these difficulties, but because these effects by definition do not exist in Si BJT's, accurate compact circuit modeling using conventional approaches is not necessarily straightforward, and warrants further attention.

F. Reliability

It is obvious that the introduction of SiGe strained layers into Si bipolar devices must impose no additional reliability risk if SiGe technology is to become commercially viable. While literature results on SiGe HBT reliability are sparse [88]–[90], results to date suggest that there is no additional risk imposed by introducing SiGe into the base, provided that thermodynamically stable films are used (there is at present no device reliability literature for metastable SiGe films, although it gives one pause for thought). Given that IBM's technology, for instance, has been fully qualified for manufacturing strongly suggests that no show-stopping reliability hurdles were encountered.

The use of epitaxial growth in place of traditional ion implantation for the formation of the intrinsic base profile can actually allow important reliability advantages to be realized in SiGe HBT's with respect to reverse-bias EB stress. Consider Fig. 20, which overlays the base doping profiles for a 60-GHz SiGe HBT [7] and a 40-GHz state-of-the-art ion-implanted Si BJT. To maintain a thin base profile using ion implantation, the combination of low-energy implantation and screen oxides are used. The resulting base profile, while thin ($<$100 nm in this case), by necessity has a peak doping concentration at the EB junction. This is problematic since band-to-band tunneling, the dominant leakage source for reverse-bias stress, depends exponentially on the electric field at the EB junction. Since the EB doping is high, the field will be high and, hence, the Si BJT is more susceptible to hot carrier damage of the EB spacer under reverse-bias stress conditions. This EB doping constraint fundamentally limits the amount of base dopant that can be introduced into a conventional implanted technology and, hence, sets a fundamental limit of achievable RF and microwave performance (via the base resistance which impacts both $f_{\max}$ and noise figure). With epitaxial growth techniques, on the other hand, the doping can be easily reduced at the EB junction, even for very heavily doping bases, strongly decreasing the reverse EB tunneling current and thus improving the device reliability of SiGe HBT's with respect to implanted base Si BJT's [25].

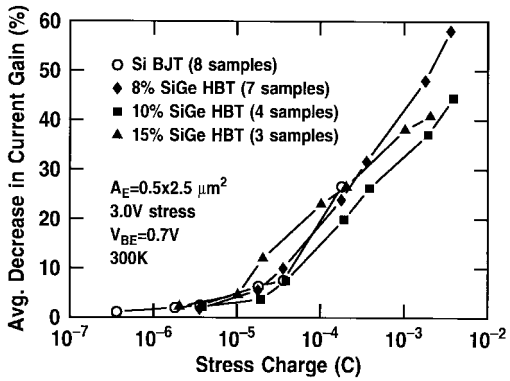

Fig. 22. Base current degradation as a function of stress charge for a variety of SiGe HBT profiles and a comparably designed Si BJT.

Fig. 21 shows the typical response of a 0.5 $\times$ 2.5 μm^2 to reverse-bias EB stress. Slight base current and, hence, β degradation associated with hot carrier damage of the EB spacer is observed, but it is well within the accepted reliability constraints for advanced bipolar technologies. Fig. 22 compares the average decrease in β at $V_{\rm BE} = 0.7$ V as a function of injected stress charge for three different Ge profiles as well as an epitaxial base Si control (with nearly identical EB doping profile). Within the statistical scatter of the data, all four profiles show similar degradation with injected charge, indicating that Ge profile shape and content has little influence on the device reliability with respect to Si. This is good news.

Finally, since the SiGe technology discussed in this paper employs a conventional five-layer CMOS metallization scheme there are no new variables to be encountered with respect to electromigration and interconnect reliability. The reliability of the other active and passive devices in this SiGe technology (refer to Table I) have not been reported, but again, it can be logically inferred that there are no serious reliability concerns in these elements since the technology has been qualified for manufacturing.

IV. Technology Issues

The previous section gave an overview of the performance advantages of SiGe HBT's. Viable RF and microwave circuit technologies obviously require more than just high-quality transistors. In this section, a number of other technology related issues are briefly addressed, including: 1) growth and film stability; 2) profile design; 3) passives; 4) transmission lines; 5) SiGe BiCMOS for system-on-a-chip; 6) manufacturability; and 7) cost. Where possible, common myths and misconceptions will be highlighted and clarified.

A. Growth Techniques, Film-Stability Issues and Ge Profile Design

There are at present a number of different SiGe growth techniques which have been used successfully around the world to realize functional SiGe HBT's, including: 1) molecular beam epitaxy (MBE) [4], [10], [12]; 2) rapid-thermal chemical-vapor deposition (RTCVD) [14]; 3) UHV/CVD [6]–[9]; 4) reduced-pressure (or atmospheric-pressure) chemical-vapor deposition (RPCVD) [19]; and 5) various other "home-built" derivatives. There is, of course, a big difference between growing a functional device and making a manufacturable technology. There are proponents for each of the growth techniques listed above, but in basic terms, for realizing a low-cost Si-processing-compatible SiGe technology, several key features are required:

1) film uniformity and control for both doping, Ge content, film thickness, and Ge profile shape must be excellent (e.g., $<5\%$ variation across the wafer) on large Si wafers (200 mm currently, and extendable to 300 mm);
2) film contaminants (e.g., C and O) must be miniscule, with excellent interface quality between the epi layer and the underlying substrate;
3) growth conditions (i.e., rate and temperature) must allow very abrupt doping transitions with large dynamic range;
4) batch wafer processing for high wafer throughput is highly desirable.

Clearly, these prerequisites are not satisfied for MBE and RTCVD (the latter essentially being a university research tool). Recent manufacturing data on UHV/CVD [25], [28] suggests that it is capable of meeting all of these requirements, but at present, published manufacturing data simply does not exist on the other growth techniques.

As mentioned above, thermodynamically stable SiGe films are a necessity for a CMOS-compatible SiGe technology since exposure to processing temperatures above the original growth temperature (typically around 600 °C) will result in film relaxation via defect generation. Obviously the presence of defects is incompatible with a high-yield low-cost technology. It has been clearly established for the present SiGe HBT technology that Si-like device yield can be achieved. Fig. 23 shows results from a typical yield monitor on a 200-mm wafer consisting of 4000 minimum geometry SiGe HBT's with an emitter area of $0.5 \times 1.0\ \mu\text{m}^2$ which have been wired in parallel. Transistor arrays which have even one bad device will show significant off-state leakage under collector–base bias, and are called "fails" (refer to the sample fail in Fig. 22).

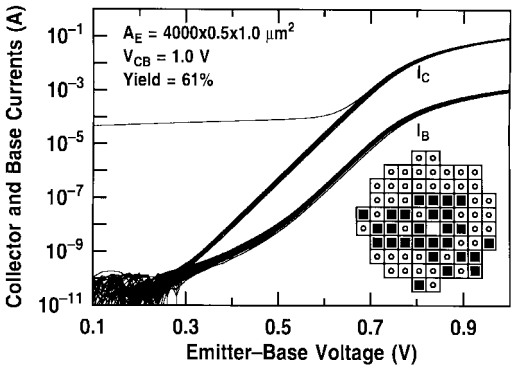

Fig. 23. 4000 transistor-chain yield for a commercial UHV/CVD SiGe HBT technology.

These results, which are in fact nearly three years old now, indicate a 61% yield on the 4000 transistor array from early manufacturing hardware. Current manufacturing lots routinely have yields in excess of 85% [28]. CMOS yields in the SiGe BiCMOS technology have been verified with aggressive 64k static random-access memory (SRAM) to be comparable to conventional Si CMOS [60]. SiGe technology using stable films can and does look like Si from a yield point of view.

Stability constraints limit the maximum (stable) Ge content to around 8%–12% (depending on the Ge shape) for base widths in the 80–100-nm range and 16%–24% for base widths in the 40–50-nm range. Misconceptions persist in the literature concerning the optimal Ge profile shape in an SiGe HBT. Many groups favor a graded-base design (e.g., see Fig. 4), while others employ constant Ge ("box") profiles. What is the best Ge profile shape? There is no simple answer, and the tradeoffs can be subtle. If we limit the discussion to manufacturable SiGe technologies employing stable Ge profiles, then we can generally say that for devices which are limited by the base transit time, it makes sense to use at least a partially graded Ge profile to induce a drift field in the base (i.e., low Ge content at the EB junction, ramped up to high Ge content at the CB junction). Base transit time-limited devices (e.g., the present SiGe technology) typically have base widths greater than 50 nm, poly-emitter contacts which have inherently high β to naturally reduce the emitter transit time, and heavily doped collectors which minimize the collector transit time. In this case, the peak Ge content can be significantly larger than for a box profile at the same stability point, and has the advantage of also improving the Early voltage. As the base width is scaled, of course, the base transit time naturally decreases, and at some point, the emitter transit time will become just as important, even in a poly-emitter technology. In this case, the box Ge profiles begin to offer a speed advantage, and since the base is already heavily doped to maintain reasonable base resistance at the thin base width, maintaining high Early voltage is relatively easy. A logical compromise at a given design point is a combination of a box profile with a linearly graded profile to form a trapezoidal Ge profile. It is interesting to note, however, that in the recent report of a very aggressive 130-GHz f_T SiGe HBT [92], the graded Ge profile still maintains a slight edge over the box profile design. These Ge shape and performance tradeoffs have

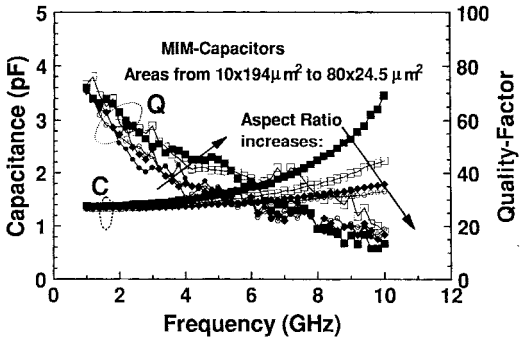

Fig. 24. Capacitance and quality factor as a function of frequency for a MIM capacitor in an SiGe technology [94].

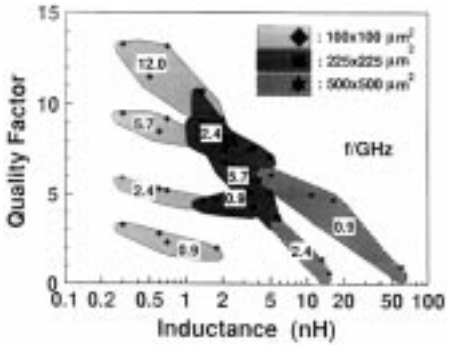

Fig. 25. Quality factor as a function of inductance at various frequencies for three different spiral inductor designs in an SiGe technology [94].

been addressed via simulation, and are discussed at length in [91].

B. Passives and Transmission Lines on Silicon

High-quality passive elements (resistors, capacitors, and inductors) which are required for both transistor biasing and monolithic matching networks are key to realizing a viable RF and microwave technology in SiGe. In contrast to popular opinion, high-quality passives are increasingly being demonstrated in Si. Precision resistors with modest sheet resistance (342 $\Omega/\square$), nearly zero-temperature coefficient, and low parasitic capacitance can be made from heavily doped polysilicon on oxide [28]. More conventional implanted resistors can be used when higher sheet resistances are required. High-quality factor (Q) precision capacitors which are made in the upper levels of the five-level metallization in a metal–insulator–metal (MIM) structure yield a 0.7-fF/μm^2 specific capacitance [93]. As can be seen in Fig. 24, Q's above 50 for 1–2-pF capacitors can be easily achieved at 2 GHz [94]. High Q inductors are the most challenging passives to build in Si, but significant progress has been made in the past several years through careful design and optimization [95], [96]. Fig. 25 shows Q as a function of inductance at practical frequencies of 900 MHz, 2.4 GHz, 5.7 GHz, and 12 GHz for several different inductor geometries. In the present SiGe technology, Q's above 5 at 900 MHz can be achieved for reasonable inductance values. At higher frequencies, Q's approaching 10 can be achieved, though at lower inductance values. Realizing inductors with both high Q and high inductance in SiGe at frequencies above 2 GHz will be challenging, but research in this area is intensifying. Recent developments in low-resistance copper interconnects potentially offer promise in this context.

For higher frequency microwave and millimeter-wave systems, low-loss transmission lines are clearly required. Advocates of III–V technologies have long pointed to the lack of suitable transmission lines in Si technology as a fundamental show stopper for realizing Si-based MMIC's. After all, there is no such thing as a semi-insulating Si substrate (at room temperature), and high-resistivity Si is difficult to make, costly, and significantly complicates conventional Si fabrication. Typical transmission-line losses on conventional Si wafers are nearly an order of magnitude higher than in GaAs, precluding any practical use. Si technologists are clever, however, and should never be underestimated. Recent work [41] indicates that thick (e.g., >10 μm) benzo–cyclo–butene (BCB) polymers, deposited directly on top of the (planar) processed SiGe wafer and followed by gold interconnect deposition can yield high-quality transmission lines in SiGe technology. Losses as low 1.5 dB/cm at 10 GHz have been achieved using this scheme, slightly higher than GaAs, but certainly competitive for MMIC's. High-quality passives can also, in principle, be realized on top of the thick BCB layer. While this post-Si BCB interconnect technology will not come for free, it clearly provides a potential path for integrating SiGe technology with future microwave and millimeter-wave transmission systems.

C. SiGe BiCMOS for System on a Chip?

Increasingly in this day and age, cost is the deciding factor in RF technology decisions. The stark reality is that system designers could care less whether the technology is GaAs or SiGe BiCMOS, or even Si CMOS, provided that it meets the system specifications and is the cheapest solution for their particular need. A cursory glance at IBM's SiGe technology clearly shows that it represents a high level of complexity. It represents the belief that a single technology is capable of satisfying many different applications and needs. Even though complex, it has been proven to be: 1) competitive in performance; 2) manufacturable; 3) high yielding; and 4) reliable. The exact cost remains to be seen. It is hard to imagine, however, that having the ability to fabricate SiGe technology in a high-volume CMOS fab using preexisting CMOS tool sets, isolation technology, and metallization would not provide some cost leverage over competing technologies. Time will tell.

There are other factors to consider as well. If, for instance, SiGe technology can be used to gain a power savings advantage by trading performance for power, the impact for a broad class of portable applications could be dramatic. In addition, one of the tremendous advantages that Si has over competing III–V technologies is its capability for high levels of integration. Witness, for instance, the case of microprocessors, which have evolved over time to include not only the processor itself, but also embedded SRAM and DRAM, multimedia signal processing, etc. Let us not forget that SiGe is truly an Si technology and is capable of similar feats.

TABLE IV
SUMMARY OF MEASURED LOAD–PULL RESULTS FOR A 40-μm^2 SiGe HBT POWER-ADDED EFFICIENCY (PAE) CELL OPERATING AT 1.8 GHz [109]. THE DEVICE WAS TUNED FOR MAXIMUM PAE

Class Operation	Bias Current	Maximum PAE	Output Power at max PAE	Gain
B	2.0 mA	69%	15.2 dBm	24.9 dB
AB	6.5 mA	60%	15.2 dBm	28.9 dB
AB	12.5 mA	52%	15.2 dBm	29.0 dB
A	25.0 mA	42%	15.2 dBm	30.1 dB

One of the great areas of debate today in the RF community is centered on the extent to which RF transceiver applications can benefit from integration. Is it possible to produce a viable transceiver "system-on-a-chip" solution? And if it can be done, is it cost-effective to do so? Cellular phones, for instance, presently consist of mostly discrete components, a primitive situation compared to digital systems. In the digital world, the merits of integration are obvious and logical, almost an unquestioned law of nature. In the RF world, however, issues such as signal isolation between the power amplifier at the output and the low-noise amplifier at the input, for instance, add significant complexity to the problem. While this remains an open issue, it does seem logical in RF transceivers to integrate the increasingly complex baseband signal processing and control functions with the high-performance mixers, oscillators, LNA's, etc. Even if the power amp, for instance, must stay on a separate IC to preserve signal isolation, single-chip integration of all other transceiver functions would appear to decrease die count, improve performance, simplify packaging, improve reliability, and presumably reduce cost. SiGe BiCMOS technology is, in principle, ideally suited to this task, since the single device technology can deliver the high-performance SiGe HBT needed for critical functions, the passives for monolithic matching, possibly the power amp (see below), as well as the Si CMOS for baseband processing and control. Only time will tell the extent to which integration plays a role in the RF transceiver market, but SiGe BiCMOS technology is clearly poised to make an impact should it become a deciding factor.

V. STATUS AND FUTURE DIRECTIONS

In the ten-and-one-half short years since the first demonstration of a functional device, SiGe technology has emerged from the research lab and entered manufacturing. In this final section, state-of-the-art circuits are reviewed, followed by a brief look at fundamental device limits and future directions.

A. The State-of-the-Art

The past three years have seen a dramatic increase in the number of practical circuits implemented in SiGe HBT technology [32]–[51]. The targeted applications range in frequency from cellular phones at 900 MHz to optical data links at 40 Gb/s. The present high-volume RF market exists at 900 MHz and 2.0 GHz. Clearly, a 70-GHz $f_{\max}$ transistor is not needed here. The emphasis instead centers on trading that raw performance to gain an advantage in some other metric over a competing technology (e.g., power dissipation, noise figure, etc.). As application frequencies continue to rise over time and these higher frequency markets develop and mature, as surely they must, SiGe HBT technology will be increasingly favored over other Si technologies because of its performance advantages. SiGe technology appears to clearly be capable of meeting performance specs at system frequencies as high as 20 GHz, and probably 40 GHz, at least for applications not requiring high-breakdown voltage.

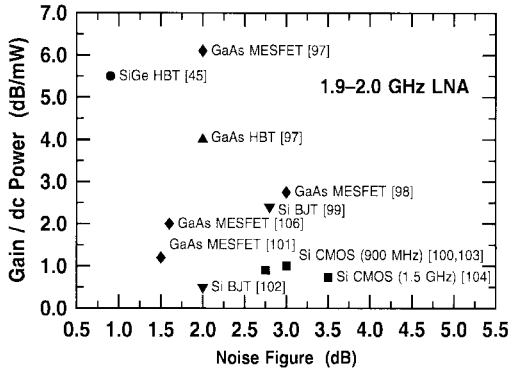

Fig. 26. Comparison of an LNA figure of merit for a variety of different device technologies. LNA gain as a function of dc power dissipation is plotted as a function of noise figure. Referenced works are enclosed in brackets.

Apples-to-apples comparisons between SiGe technology and other competing technologies are difficult to make for various reasons, but as an example, consider Fig. 26, which compares LNA's in the critical 2.0-GHz RF band. As a figure of merit, the ratio of LNA gain to power dissipation is plotted as a function of noise figure for LNA's built from SiGe HBT's, GaAs MESFET's, Si BJT's, GaAs HBT's, and Si CMOS [45], [97]–[106]. The desirable LNA design point in this figure is the upper left, with high gain per unit power dissipation operating at very low noise figure. While comparisons such as this must be taken with a grain of salt, clearly SiGe HBT's offer competitive performance compared to existing (published) LNA's. This SiGe HBT LNA achieves an impressive 0.95 dB $\mathrm{NF}_{\min}$ and 10.5-dB gain at 2.5 mW with an input third-order intercept point (IP3) of -4.5 dBm [45].

Contrary to popular opinion, SiGe HBT's are capable of delivering competitive power amplifiers at 900 MHz and 1.8 GHz [107]–[109]. Table IV shows representative load–pull results at 1.8 GHz off a single 40-μm^2 power cell from the present SiGe HBT technology in various classes of operation. These results are shown for the high-breakdown ($BV_{\mathrm{CEO}} = 5.3$ V) transistor (refer to Table I). In Class B operation, for instance, this single 40-μm^2 power cell delivers 0.83-mW/μm^2 power density and 69% efficiency when tuned for maximum efficiency, and 1.10-mW/μm^2 power density and 61% effi-

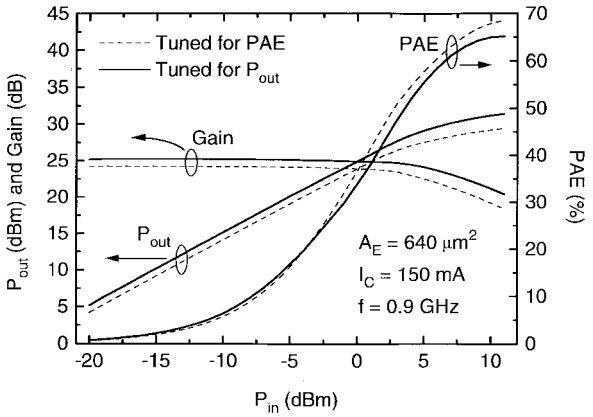

Fig. 27. Load–pull data showing output power ($P_{\rm out}$), gain, and PAE as a function of input power for a 640-μm^2 SiGe HBT power amplifier operating at 900 MHz. Results are shown for tuning to achieve both maximum efficiency and maximum output power [109].

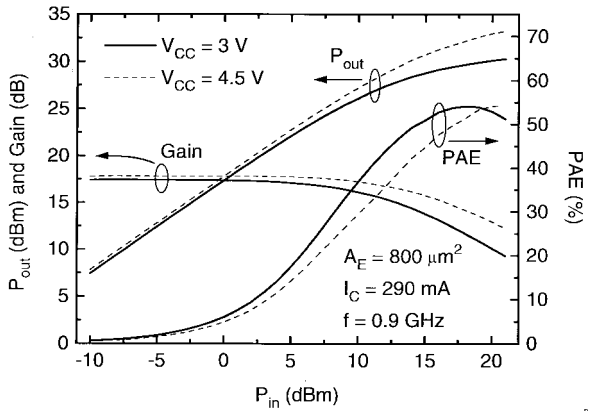

Fig. 28. Load–pull data showing output power ($P_{\rm out}$), gain, and PAE as a function of input power for a 800-μm^2 SiGe HBT power amplifier operating at 900 MHz under a bias of both 3.0 and 4.5 V [109].

ciency when tuned for maximum power output [109]. These efficiencies and power densities compare favorably with both GaAs HBT results (50% efficiency and 0.60 mW/μm^2) and GaAs MESFET results (65% efficiency and 0.15 mW/μm^2). The 33-mW output power of the single power cell is obviously too small to be of practical use in transceivers. Impressive results from upscaled versions of this single cell have recently been reported [109]. Load–pull data for a 640-μm^2 SiGe HBT power amplifier operating at 900 MHz is shown in Fig. 27 and indicates that when tuned for maximum output power, this SiGe HBT can deliver 1.25 W (1.97 mW/μm^2) with excellent efficiency (65%) and high gain (25 dB). Results for an 800-μm^2 SiGe HBT power amplifier are shown in Fig. 28, and when biased at 4.5 V delivers an output power of 2.0 W (2.5 mW/μm^2) at greater than 50% efficiency, which is competitive for cellular applications.

B. Fundamental Limits and Future Directions

Key to the long-term success of any device technology is the potential for sustained performance improvements over time.

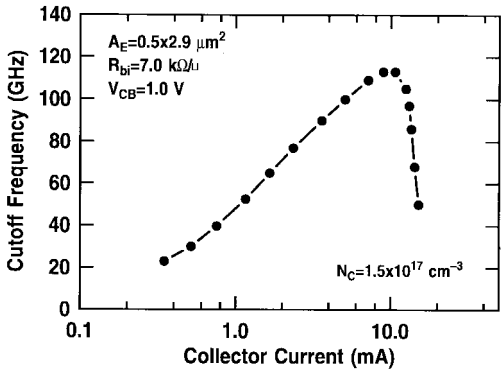

Fig. 29. Cutoff frequency as a function of bias current for an aggressively designed SiGe HBT.

This has indeed been the case for SiGe HBT's. How high will f_T go in SiGe HBT's? As discussed by Johnson 33 years ago [110], there is a fundamental reciprocal relationship between maximum achievable f_T and the $BV_{\rm CEO}$ of a transistor. SiGe helps to alleviate this constraint somewhat by introducing an additional degree of freedom (effectively decoupling the base doping from β and f_T), but the gain is modest. The SiGe technology described in this paper has an $f_T BV_{\rm CEO}$ product of 158 and 143 GHz V, for the low- and high-breakdown HBT's, respectively, not far from the Johnson limit of about 170–180-GHz V. SiGe HBT's with f_T's above 100 GHz (see Fig. 29) were demonstrated in nonself-aligned device structures in 1993 [10], [11], and the current record sits at 130 GHz [92]. The record f_T for a self-aligned SiGe HBT is 95 GHz [31], [111]. It seems reasonable to expect f_T's in excess of 150 GHz for nonself-aligned devices, and 120 GHz in self-aligned devices in the near future, although $BV_{\rm CEO}$ will clearly be less than 2.0 V. Given the trend in portable communications systems, the devices may still prove useful in certain applications even with their low $BV_{\rm CEO}$.

Placing too much emphasis on the maximum achievable f_T in SiGe HBT's can be misleading, however, since $f_{\rm max}$ is a far more relevant metric for real RF and microwave circuits. For high $f_{\rm max}$, one needs a self-aligned device structure with minimal external parasitics, and while one obviously still needs high f_T, the Johnson limit is not so fundamental in this context. In the realm of $f_{\rm max}$, structural and process innovation is king, and room for improvement still remains. The record $f_{\rm max}$ for SiGe HBT's is currently 160 GHz [112], although this technology is not compatible with low-cost Si fabrication. The highest $f_{\rm max}$ in an Si-compatible technology is 74 GHz at present [22]. It seems reasonable to expect this number to climb into the 110–120-GHz range for manufacturable SiGe technologies using stable Ge profiles, provided care is taken in profile optimization [91]. Evolution to *in-situ* doped poly-emitter contacts, and metal base contacts may be required.

The most serious constraint in the further scaling of the vertical profile in SiGe HBT's for higher performance is the minimization of boron out-diffusion with the annealing steps needed for extrinsic base implant activation and emitter drive-in. A recent discovery which may prove fruitful in this context is that the introduction of small amounts of C (perhaps as low as $<$0.05%) into the base of an SiGe HBT strongly suppresses

boron out-diffusion [113]. If it turns out that the addition of C has no serious consequences on performance and reliability, this (simple) technique may allow a straightforward migration to significantly higher frequency response since it would relax the thermal cycle constraints in the fabrication sequence. This remains an active area of research.

VI. Conclusion

It has been argued throughout this paper that SiGe is an idea whose time has come. The original motivation for developing SiGe technology is beautifully simple: let us combine transistor performance which is competitive with the III–V technologies with the processing maturity, integration levels, yield, and, hence, cost commonly associated with conventional Si fabrication. What once seemed like a dream is now reality. Ten-and-one-half years have passed since the first demonstration of a functional SiGe HBT, and since that time progress has been very rapid, yielding a fully qualified SiGe HBT technology on 200-mm wafers today. State-of-the-art SiGe HBT's can deliver competitive performance, achieving f_T in excess of 50 GHz, $f_{\max}$ in excess of 70 GHz, minimum noise figure below 0.7 dB at 2.0 GHz, $1/f$ noise corner frequencies below 500 Hz, excellent radiation hardness, competitive power amplifiers, and reliability comparable to Si. A clear scaling path to even higher performance levels exists. A host of record-setting digital, analog, RF, and microwave circuits have been demonstrated in the past several years using SiGe HBT's, and recent work on passives and transmission lines on Si suggest a migratory path to Si-based MMIC's is possible. The combination of SiGe HBT's with advanced Si CMOS to form an SiGe BiCMOS technology represents a unique opportunity for Si-based RF system-on-a-chip solutions. Key to the successful penetration and long-term success of SiGe HBT technology in the RF and microwave marketplace will lie in its cost/performance, and while the picture has not yet been fully painted, the future for SiGe appears bright.

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References

[1] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers—I: Misfit dislocations in layers," *J. Crystal Growth*, vol. 27, pp. 118–125, 1974.

[2] ———, "Defects in epitaxial multilayers—II: Dislocation pile-ups, threading dislocations, slip lines and cracks," *J. Crystal Growth*, vol. 32, pp. 265–273, 1975.

[3] S. R. Stiffler, J. H. Comfort, C. L. Stanis, D. L. Harame, and E. de Frésart, "The thermal stability of SiGe films deposited by ultrahigh-vacuum chemical vapor deposition," *J. Appl. Phys.*, vol. 70, pp. 1416–1420, 1991. See also, "Erratum," *J. Appl. Phys.*, vol. 70, p. 7194, 1991.

[4] S. S. Iyer, G. L. Patton, S. L. Delage, S. Tiwari, and J. M. C. Stork, "Silicon-germanium base heterojunction bipolar transistors by molecular beam epitaxy," in *Tech. Dig. Int. Electron Device Meeting*, 1987, pp. 874–876.

[5] G. L. Patton, S. S. Iyer, S. L. Delage, S. Tiwari, and J. M. C. Stork, "Silicon–germanium-base heterojunction bipolar transistors by molecular beam epitaxy," *IEEE Electron Device Lett.*, vol. 9, pp. 165–167, Apr. 1988.

[6] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbé, G. J. Scilla, E. de Fresart, J. M. C. Stork, J. Y.-C. Sun, D. L. Harame, and J. Burghartz, "75 GHz f_T SiGe base heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 11, pp. 171–173, Apr. 1990.

[7] J. H. Comfort, G. L. Patton, J. D. Cressler, W. Lee, E. F. Crabbé, B. S. Meyerson, J. Y.-C. Sun, J. M. C. Stork, P.-F. Lu, J. N. Burghartz, J. Warnock, K. Kenkins, K.-Y. Toh, M. D'Agostino, and G. Scilla, "Profile leverage in a self-aligned epitaxial Si or SiGe-base bipolar technology," in *Tech. Dig. Int. Electron Device Meeting*, 1990, pp. 21–24.

[8] D. L. Harame, E. F. Crabbé, J. D. Cressler, J. H. Comfort, J. Y.-C. Sun, S. R. Stiffler, E. Kobeda, J. N. Burghartz, M. M. Gilbert, J. Malinowski, and A. J. Dally, "A high-performance epitaxial SiGe-base ECL BiCMOS technology," in *Tech. Dig. Int. Electron Device Meeting*, 1992, pp. 19–22.

[9] D. L. Harame, J. M. C. Stork, B. S. Meyerson, K. Y.-J. Hsu, J. Cotte, K. A. Jenkins, J. D. Cressler, P. Restle, E. F. Crabbé, S. Subbanna, T. E. Tice, B. W. Scharf, and J. A. Yasaitis, "Optimization of SiGe HBT technology for high speed analog and mixed-signal applications," in *Tech. Dig. Int. Electron Device Meeting*, 1993, pp. 71–74.

[10] E. Kasper, A. Gruhle, and H. Kibbel, "High speed SiGe-HBT with very low base sheet resistivity," in *Tech. Dig. Int. Electron Device Meeting*, 1993, pp. 79–81.

[11] E. F. Crabbé, B. S. Meyerson, J. M. C. Stork, and D. L. Harame, "Vertical profile optimization of very high frequency epitaxial Si- and SiGe-base bipolar transistors," in *Tech. Dig. Int. Electron Device Meeting*, 1993, pp. 83–86.

[12] A. Schuppen, A. Gruhle, U. Erben, H. Kibbel, and U. Konig, "Multi-emitter finger SiGe HBT's with $f_{\max}$ up to 120 GHz," in *Tech. Dig. Int. Electron Device Meeting*, 1994, pp. 377–380.

[13] D. L. Harame, K. Schonenberg, M. Gilbert, D. Nguyen-Ngoc, J. Malinowski, S.-J. Jeng, B. S. Meyerson, J. D. Cressler, R. Groves, G. Berg, K. Tallman, K. Stein, G. Hueckel, C. Kermarrec, T. Tice, G. Fitzgibbons, K. Walter, D. Colavito, T. Houghton, N. Greco, T. Kebede, B. Cunningham, S. Subbanna, J. H. Comfort, and E. F. Crabbé, "A 200 mm SiGe-HBT technology for wireless and mixed-signal applications," in *Tech. Dig. Int. Electron Device Meeting*, 1994, pp. 437–440.

[14] C. A. King, J. L. Hoyt, C. M. Gronet, J. F. Gibbons, M. P. Scott, and J. Turner, "$Si/Si_{1-x}/Ge_x$ heterojunction bipolar transistors produced by limited reaction processing," *IEEE Electron Device Lett.*, vol. 10, pp. 52–54, Feb. 1989.

[15] J. N. Burghartz, J. H. Comfort, G. L. Patton, J. D. Cressler, B. S. Meyerson, J. M. C. Stork, J. Y.-C. Sun, G. Scilla, J. Warnock, K. Jenkins, K.-Y. Toh, D. L. Harame, and S. R. Mader, "Sub-30 ps ECL circuits using high f_T Si and SiGe epitaxial SEEW transistors," in *Tech. Dig. Int. Electron Device Meeting*, 1990, pp. 297–300.

[16] J. H. Comfort, E. F. Crabbé, J. D. Cressler, W. Lee, J. Y.-C. Sun, J. Malinowski, M. D-Agostino, J. N. Burghartz, J. M. C. Stork, and B. S. Meyerson, "Single crystal emitter cap for epitaxial Si- and SiGe base transistors," in *Tech. Dig. Int. Electron Device Meeting*, 1991, pp. 857–860.

[17] A. Gruhle, H. Kibbel, U. König, U. Erben, and E. Kasper, "MBE-grown Si/SiGe HBT's with high β, f_T, and $f_{\max}$," *IEEE Electron Device Lett.*, vol. 13, pp. 206–208, Apr. 1992.
[18] E. F. Crabbé, J. H. Comfort, J. D. Cressler, J. Y.-C. Sun, and J. M. C. Stork, "High-low polysilicon-emitter SiGe-base bipolar transistors," *IEEE Electron Device Lett.*, vol. 14, pp. 478–480, Oct. 1993.
[19] M. Hong, E. de Fresart, J. Steele, A. Zlotnicka, C. Stein, G. Tam, M. Racanelli, L. Knoch, Y. C. See, and K. Evans, "High-performance epitaxial base bipolar transistors produced by a reduced-pressure CVD reactor," *IEEE Electron Device Lett.*, vol. 14, pp. 450–452, Sept. 1993.
[20] D. Harame, L. Larson, M. Case, K. Kovacic, S. Voinigescu, T. Tewksbury, D. Nguyen-Ngoc, K. Stein, J. D. Cressler, S.-J. Jeng, J. Malinowski, R. Groves, E. Eld, D. Sunderland, D. Rensch, M. Gilbert, K. Schonenberg, D. Ahlgren, S. Rosenbaum, J. Glenn, and B. Meyerson, "SiGe HBT technology: Device and application issues," in *Tech. Dig. Int. Electron Device Meeting*, 1995, pp. 731–734.
[21] F. Sato, T. Hashimoto, T. Tatsumi, M. Soda, H. Tezuka, T. Sazaki, and T. Tashiro, "A self-aligned SiGe base bipolar technology using cold wall UHV/CVD and its application for optical communications IC's," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1995, pp. 82–88.
[22] T. Meister, H. Schäfer, M. Franosch, W. Molzer, K. Aufinger, U. Scheler, C. Walz, M. Stolz, S. Boguth, and J. Böck, "SiGe base bipolar technology with 74 GHz $f_{\max}$ and 11 ps gate delay," in *Tech. Dig. Int. Electron Device Meeting*, 1995, pp. 739–742.
[23] A. Pruijmboom, D. Terpstra, C. Timmering, W. deBoer, M. Theunissen, J. Slotboom, R. Hueting, and J. Hageraats, "Selective-epitaxial base technology with 14 ps ECL-gate delay for low power wide-band communications systems," in *Tech. Dig. Int. Electron Device Meeting*, 1995, pp. 747–750.
[24] S. Lombardo, A. Pinto, A. Raineri, P. Ward, and S. Campisano, "Si/GeSi HBT's with GeSi base formed by high dose Ge implantation into Si," in *Tech. Dig. Int. Electron Device Meeting*, 1995, pp. 1019–1021.
[25] D. Ahlgren, M. Gilbert, D. Greenberg, S.-J. Jeng, J. Malinowski, D. Nguyen-Ngoc, K. Schonenberg, K. Stein, D. Sunderland, R. Groves, K. Walter, G. Hueckel, D. Colavito, G. Freeman, D. Harame, and B. Meyerson, "Manufacturability demonstration of an integrated SiGe HBT technology for the analog and wireless marketplace," in *Tech. Dig. Int. Electron Device Meeting*, 1996, pp. 859–862.
[26] A. Schüppen, H. Dietrich, S. Gerlach, and J. Arndt, "SiGe technology and components for mobile communications systems," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1996, pp. 130–133.
[27] M. Kondo, K. Oda, E. Ohue, H. Shimamoto, M. Tanabe, T. Onai, and K. Washio, "Sub-10 fJ ECL/68 μA 4.7 GHz divider ultra-low-power SiGe base bipolar transistors with a wedge-shaped CVD-SiO_2 isolation structure and a BPSG-refilled trench," in *Tech. Dig. Int. Electron Device Meeting*, 1996, pp. 245–248.
[28] D. Ahlgren, G. Freeman, S. Subbanna, R. Groves, D. Greenberg, J. Malinowski, D. Nguyen-Ngoc, S. Jeng, K. Stein, K. Schonenberg, D. Kiesling, B. Martin, S. Wu, D. Harame, and Meyerson, "A SiGe HBT BiCMOS technology for mixed-signal RF applications," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1997, pp. 195–197.
[29] R. Götzfried, F. Beiswanger, and S. Gerlach, "Design of RF integrated circuits using SiGe bipolar technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1997, pp. 51–56.
[30] E. de Berranger, S. Brodnar, A. Chantre, J. Kirtsch, A. Monroy, A. Granier, M. Laurens, J. L. Regolini, and M. Moulis, "Integration of SiGe heterojunction bipolar transistors in a 200 mm industrial BiCMOS technology," *Thin Solid Films*, vol. 294, pp. 250–253, 1997.
[31] K. Washio, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, and T. Onai, "95 GHz f_T self-aligned selective-epitaxial SiGe HBT's with SMI electrodes," presented at the IEEE Int. Solid-State Circuits Conf., Feb. 1998.
[32] M. Soda, H. Tezuka, F. Sato, T. Hashimoto, S. Nakamura, T. Tatsumi, and T. Tashiro, "Si-analog IC's for 20 Gb/s optical receiver," in *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 1994, pp. 170–171.
[33] T. Hashimoto, F. Sato, M. Soda, H. Tezuka, T. Suzuki, T. Tatsumi, and T. Tashiro, "SiGe bipolar IC's for a 20 Gb/s optical transmitter," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1994, pp. 167–170.
[34] F. Sato, T. Hashimoto, T. Tatsumi, and T. Tashiro, "Sub-20 ps ECL circuits with high-performance super self-aligned selectively grown SiGe base (SSSB) bipolar transistors," *IEEE Trans. Electron Devices*, vol. 42, pp. 483–488, Mar. 1995.
[35] M. Case, L. Larson, D. Rensch, S. Rosenbaum, S. Knorr, D. Harame, and B. Meyerson, "A 23 GHz static 1/128 frequency divider implemented in a manufacturable Si/SiGe HBT process," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1995, pp. 121–123.
[36] W. Gao, W. Snelgrove, T. Varelas, S. Kovacic, and D. Harame, "A 5-GHz SiGe HBT return-to-zero comparator," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1995, pp. 166–169.
[37] J. Glenn, R. Poisson, M. Case, D. Harame, and B. Meyerson, "12-GHz Gilbert mixers using a manufacturable Si/SiGe epitaxial-base bipolar technology," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1995, pp. 186–189.
[38] H. Schumacher, U. Erben, A. Gruhle, H. Kibbel, and U. König, "A 3 V supply voltage, DC-18 GHz SiGe HBT wide-band amplifier," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1995, pp. 190–193.
[39] A. Gruhle, A. Schüppen, U. König, U. Erben, and H. Schumacher, "Monolithic 26 GHz and 40 GHz VCO's with SiGe heterojunction bipolar transistors," in *Tech. Dig. Int. Electron Device Meeting*, 1995, pp. 725–728.
[40] F. Sato, H. Tezuka, M. Soda, T. Hashimoto, T. Suzaki, T. Tatsumi, T. Morikawa, and T. Tashiro, "The optical terminal IC: A 2.4 Gb/s receiver and a 1:16 demultiplexer in one chip," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1995, pp. 162–165.
[41] L. Larson, M. Case, S. Rosenbaum, D. Rensch, P. MacDonald, M. Matloubian, M. Chen, D. Harame, J. Malinowski, B. Meyerson, M. Gilbert, and S. Maas, "Si/SiGe HBT technology for low-cost monolithic microwave integrated circuits," in *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 1996, pp. 80–81.
[42] F. Sato, H. Tezuka, M. Soda, T. Hashimoto, T. Suzaki, T. Tatsumi, T. Morikawa, and T. Tashiro, "A 2.4 Gb/s receiver and a 1:16 demultiplexer in one chip using a super self-aligned selectively grown SiGe base (SSSB) bipolar transistor," *IEEE J. Solid-State Circuits*, vol. 1451–1457, Oct. 1996.
[43] M. Soyuer, J. Burghartz, H. Ainspan, K. Jenkins, P. Xiao, A. Shahani, M. Dolan, and D. Harame, "An 11 GHz 3 V SiGe voltage-controlled oscillator with integrated resonator," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1996, pp. 169–1172.
[44] R. Götzfried, T. Itoh, J. F. Luy, and H. Schumacher, "Zero power consumption Si/SiGe HBT SPDT T/R antenna switch," in *Tech. Dig. IEEE MTT-S Int. Microwave Symp.*, 1996, pp. 651–653.
[45] J. Long, M. Copeland, S. Kovacic, D. Malhi, and D. Harame, "RF analog and digital circuits in SiGe technology," in *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 1996, pp. 82–83.
[46] W. Gao, W. Snelgrove, and S. Kovacic, "A 5-GHz SiGe HBT return-to-zero comparator for RF A/D conversion," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1502–1506, 1996.
[47] M. Soda, T. Morikawa, S. Shioiri, H. Tezuka, F. Sato, T. Tatsumi, K. Emura, T. Tashiro, "A 1 Gb/s 8-channel array OEIC with SiGe photdetectors," in *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 1997, pp. 120–121.
[48] M. Wurzer, T. Miester, H. Schäfer, H. Knapp, J. Böck, R. Stengl, K. Aufinger, M. Franosch, M. Rest, M. Möller, H.-M. Rein, and A. Felder, "42 GHz static frequency divider in Si/SiGe bipolar technology," in *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 1997, pp. 122–123.
[49] P. Xiao, K. Jenkins, M. Soyuer, H. Ainspan, J. Burghartz, H. Shin, M. Dolan, and D. Harame, "A 4 b 8 GSample/s A/D converter in SiGe bipolar technology," in *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 1997, pp. 124–125.
[50] S. Shiori, M. Soda, R. Morikawa, T. Hashimoto, F. Sato, and K. Emura, "A 10 Gb/s SiGe bipolar framer/demultiplexer for SDH system," presented at the IEEE Int. Solid-State Circuits Conf., Feb. 1998.
[51] T. Masuda, K.-I. Ohhata, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, T. Onai, and K. Washio, "40 Gb/s analog IC chipset for optical receiver using SiGe HBT's," presented at the IEEE Int. Solid-State Circuits Conf., Feb. 1998.
[52] R. People, "Physics and applications of Ge_xSi_{1-x}/Si strained layer heterostructures," *IEEE J. Quantum Electron.*, vol. QE-22, p. 1696, Oct. 1986.
[53] G. L. Patton, J. M. C. Stork, J. H. Comfort, E. F. Crabbé, B. S. Meyerson, D. L. Harame, and J. Y.-C. Sun, "SiGe-base heterojunction bipolar transistors: Physics and design issues," in *Tech. Dig. Int. Electron Device Meeting*, 1990, pp. 13–16.
[54] B. Meyerson, "UHV/CVD growth of Si and SiGe alloys: Chemistry, physics, and device applications," *Proc. IEEE*, vol. 80, p. 1592, June 1992.
[55] J. D. Cressler, D. L. Harame, J. H. Comfort, J. M. C. Stork, B. S. Meyerson, and T. E. Tice, "Silicon-germanium heterojunction bipolar technology: The next leap in silicon?," *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 1994, pp. 24–27.
[56] C. Kermarrec, T. Tewksbury, G. Dawe, R. Baines, B. Meyerson, D. Harame, and M. Gilbert, "SiGe HBT's reach the microwave and millimeter-wave frontier," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1994, pp. 155–162.

[57] J. D. Cressler, "Re-engineering silicon: Si-Ge heterojunction bipolar technology," *IEEE Spectrum Mag.*, pp. 49–55, Mar. 1995.
[58] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbé, J. Y.-C. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors: Part I—Materials, physics, and circuits," *IEEE Trans. Electron Devices*, vol. 40, pp. 455–468, Mar. 1995.
[59] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbé, J. Y.-C. Sun, B. S. Meyerson, and T. Tice, "Si/SiGe epitaxial-base transistors: Part II—Process integration and analog applications," *IEEE Trans. Electron Devices*, vol. 40, pp. 469–482, Mar. 1995.
[60] D. L. Harame, "High-performance BiCMOS process integration: Trends, issues, and future directions," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1997, pp. 36–43.
[61] B. S. Meyerson, "Low-temperature silicon epitaxy by ultrahigh vacuum/chemical vapor deposition," *Appl. Phys. Lett.*, vol. 48, pp. 797–799, 1986.
[62] P.-F. Lu, "Low-frequency noise in self-aligned bipolar transistors," *J. Appl. Phys.*, vol. 62, pp. 1335–1339, 1987.
[63] L. Vempati, J. D. Cressler, J. Babcock, R. Jaeger, and D. Harame, "Low-frequency noise in UHV/CVD Si- and SiGe-base bipolar transistors," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1995, pp. 125–128.
[64] J. D. Cressler, L. Vempati, J. A. Babcock, R. C. Jaeger, and D. L. Harame, "Low-frequency noise characteristics of UHV/CVD epitaxial Si- and SiGe-base bipolar transistors," *IEEE Electron Device Lett.*, vol. 17, pp. 13–15, Jan. 1996.
[65] L. Vempati, J. D. Cressler, J. Babcock, R. Jaeger, and D. Harame, "Low-frequency noise in UHV/CVD epitaxial Si- and SiGe-base bipolar transistors," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1458–1467, Oct. 1996.
[66] D. Costa, M. N. Tutt, A. Khatibzadeh, and D. Pavlidis, "Tradeoff between $1/f$ noise and microwave performance in AlGaAs/GaAs heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 41, pp. 1347–1350, Aug. 1994.
[67] T. G. M. Kleinpenning and A. J. Holden, "$1/f$ noise in n-p-n GaAs/AlGaAs heterojunction bipolar transistors: Impact of intrinsic transistor and parasitic series resistance," *IEEE Trans. Electron Devices*, vol. 40, pp. 1148–1153, June 1993.
[68] H. A. W. Markus and T. G. M. Kleinpenning, "Low-frequency noise in polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. 42, pp. 720–727, Apr. 1995.
[69] D. S. Quon, G. J. Sonek, and G. P. Li, "$1/f$ noise characterization of base current and emitter interfacial oxide breakup in n-p-n polyemitter bipolar transistors," *IEEE Electron Device Lett.*, vol. 15, pp. 430–432, Oct. 1994.
[70] H. Schumacher, U. Erben, and A. Gruhle, "Low-noise performance of SiGe heterojunction bipolar transistors," in *Tech. Dig. IEEE MTT-S Int. Microwave Symp.*, 1994, pp. 1167–1170.
[71] W. E. Ansley, J. D. Cressler, and D. M. Richey, "Base profile optimization for minimum noise figure in advanced UHV/CVD SiGe HBT's," this issue, pp. 652–659.
[72] J. A. Babcock, J. D. Cressler, L. S. Vempati, S. D. Clark, R. C. Jaeger, and D. L. Harame, "Ionizing radiation tolerance and low-frequency noise degradation in UHV/CVD SiGe HBT's," *IEEE Electron Device Lett.*, vol. 16, pp. 351–353, Aug. 1995.
[73] ———, "Ionizing radiation tolerance of high-performance SiGe HBT's grown by UHV/CVD," *IEEE Trans. Nucl. Sci.*, vol. 42, pp. 1558–1567, Dec. 1995.
[74] J. Roldán, W. E. Ansley, J. D. Cressler, S. D. Clark, and D. Nguyen-Ngoc, "Neutron radiation tolerance of advanced UHV/CVD SiGe HBT BiCMOS technology," *IEEE Trans. Nucl. Sci.*, vol. 44, pp. 1965–1973, Dec. 1997.
[75] J. Roldán, G. F. Niu, W. E. Ansley, J. D. Cressler, and S. D. Clark, "An investigation of the spatial location of proton-induced traps in SiGe HBT's," to be presented at the Nucl. Space Radiation Effects Conf., 1998.
[76] H. Ohyama, J. Vanhellemont, Y. Takami, K. Hayama, H. Sunaga, J. Poortmans, and M. Caymax, "Degradation of SiGe epitaxial heterojunction bipolar transistors by 1-MeV fast neutrons," *IEEE Trans. Nucl. Sci.*, vol. 42, pp. 1550–1557, Dec. 1995.
[77] E. F. Crabbé, G. L. Patton, J. M. C. Stork, J. H. Comfort, B. S. Meyerson, and J. Y.-C. Sun, "The low temperature operation of Si and SiGe bipolar transistors," in *Tech. Dig. Int. Electron Device Meeting*, 1990, pp. 17–20.
[78] J. D. Cressler, J. H. Comfort, E. F. Crabbé, G. L. Patton, W. Lee, J. Y.-C. Sun, J. M. C. Stork, and B. S. Meyerson, "Sub 30-ps ECL circuit operation at liquid nitrogen temperature using self-aligned epitaxial SiGe-base bipolar transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 166–168, Apr. 1991.
[79] J. D. Cressler, J. H. Comfort, E. F. Crabbé, G. L. Patton, J. M. C. Stork, J. Y.-C. Sun, and B. S. Meyerson, "On the profile design and optimization of epitaxial Si- and SiGe-base bipolar technology for 77 K applications—Part I: Transistor dc design considerations," *IEEE Trans. Electron Devices*, vol. 40, pp. 525–541, Mar. 1993.
[80] J. D. Cressler, E. F. Crabbé, J. H. Comfort, J. M. C. Stork, and J. Y.-C. Sun, "On the profile design and optimization of epitaxial Si- and SiGe-base bipolar technology for 77 K applications—Part II: Circuit performance issues," *IEEE Trans. Electron Devices*, vol. 40, pp. 542–556, Mar. 1993.
[81] J. D. Cressler, E. F. Crabbé, J. H. Comfort, J. Y.-C. Sun, and J. M. C. Stork, "An epitaxial emitter cap SiGe-base bipolar technology for liquid nitrogen temperature operation," *IEEE Electron Device Lett.*, vol. 15, pp. 472–474, Nov. 1994.
[82] J. W. Slotboom, G. Streutker, A. Pruijmboom, and D. J. Gravesteijn, "Parasitic energy barriers in SiGe HBT's," *IEEE Electron Device Lett.*, vol. 12, pp. 486–488, Sept. 1991.
[83] E. F. Crabbé, J. D. Cressler, G. L. Patton, J. M. C. Stork, J. H. Comfort, and J. Y.-C. Sun, "Current gain rolloff in graded-base SiGe heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 14, pp. 193–195, Apr. 1993.
[84] S. L. Salmon, J. D. Cressler, R. C. Jaeger, and D. L. Harame, "The impact of Ge profile shape on the operation of SiGe HBT precision voltage references," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1997, pp. 100–103.
[85] A. J. Joseph, J. D. Cressler, R. C. Jaeger, D. Richey, and D. L. Harame, "Neutral base recombination in advanced SiGe HBT's and its impact on the temperature characteristics of precision analog circuits," in *Tech. Dig. IEEE Int. Electron Device Meeting*, 1995, pp. 755–758.
[86] A. J. Joseph, J. D. Cressler, D. M. Richey, R. C. Jaeger, and D. L. Harame, "Neutral base recombination and its influence on the temperature dependence of early voltage and current-gain early voltage product in UHV/CVD SiGe heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 404–413, Mar. 1997.
[87] A. J. Joseph, J. D. Cressler, D. Richey, and D. Harame, "Impact of profile scaling on high-injection barrier effects in advanced UHV/CVD SiGe HBT's," in *Tech. Dig. IEEE Int. Electron Device Meeting*, 1996, pp. 253–256.
[88] K. Liao, R. Rief, and T. Kamins, "Effect of current and voltage stress on the dc characteristics of SiGe-base heterojunction bipolar transistors," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1994, pp. 209–212.
[89] J. A. Babcock, J. D. Cressler, L. Vempati, A. Joseph, and D. Harame, "Correlation of low-frequency noise and emitter-base reverse-bias stress in epitaxial Si-and SiGe-base bipolar transistors," *Tech. Dig. IEEE Int. Electron Device Meeting*, 1995, pp. 357–360.
[90] A. Neugroschel, C.-T. Sah, J. M. Ford, J. Steele, R. Tang, and C. Stein, "Comparison of time-to-failure of GeSi and Si bipolar transistors," *IEEE Electron Device Lett.*, vol. 17, pp. 211–213, Apr. 1996.
[91] D. M. Richey, J. D. Cressler, and A. J. Joseph, "Scaling issues and Ge profile optimization in advanced UHV/CVD SiGe HBT's," *IEEE Trans. Electron Devices*, vol. 44, pp. 431–440, Mar. 1997.
[92] K. Oda, E. Ohue, M. Tanabe, H. Shimamoto, T. Onai, and K. Washio, "130 GHz f_T SiGe HBT technology," in *Tech. Dig. Int. Electron Device Meeting*, 1997, pp. 791–794.
[93] K. Stein, J. Kocis, G. Hueckel, E. Eld, T. Bartush, R. Groves, N. Greco, D. Harame, and T. Tewksbury, "High reliability metal insulator metal capacitors for silicon-germanium analog applications," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, 1997, pp. 191–194.
[94] J. Burghartz, M. Soyuer, K. Jenkins, M. Kies, M. Dolan, K. Stein, J. Malinowski, and D. Harame, "Integrated RF components in a SiGe bipolar technology," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1440–1445, Sept. 1997.
[95] J. Burghartz, M. Soyuer, K. Jenkins, and M. Hulvey, "High-Q inductors in standard silicon interconnect technology and its application to an integrated RF power amplifier," in *Tech. Dig. Int. Electron Device Meeting*, 1995, pp. 1015–1017.
[96] J. Burghartz, D. Edelstein, M. Soyuer, H. Ainspan, and K. Jenkins, "RF circuit design aspects of spiral inductors in silicon," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 1998, pp. 246–247.
[97] K. Kobayashi *et al.*, "Ultra-low dc power GaAs HBT S- and C-band low-noise amplifiers for portable wireless communications," *IEEE Trans. Microwave Theory Tech*, vol. 43, pp. 3055–3061, Dec. 1995.
[98] S. Harra *et al.*, "Miniature low-noise variable MMIC amplifiers with low power consumption for L-band portable communications applications," in *Tech. Dig. IEEE MTT-S Int. Microwave Symp.*, 1991, pp. 67–70.

[99] J. Long and M. Copeland, "A 1.9-GHz low-voltage silicon bipolar receiver front-end for wireless personal communications systems," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1438–1448, Dec. 1995.
[100] A. Karanicolas *et al.*, "A 2.7 V 900 MHz CMOS LNA and mixer," in *Tech. Dig. IEEE Int. Solid-State Circuits Conf.*, 1996, pp. 50–51.
[101] K. Cioffi, "Monolithic L-band amplifiers operating at milliwatt dc power consumption," in *Tech. Dig. IEEE MMWMCS*, 1992, pp. 9–12.
[102] H. Takeuchi *et al.*, "A Si wide-band amplifier MMIC amplifier family for L–S band consumer product applications," in *Tech. Dig. IEEE MTT-S Int. Microwave Symp.*, 1991, pp. 1283–1284.
[103] J.-J. Zhou and D. Allstot, "A fully-integrated CMOS 900 MHz LNA utilizing monolithic trasnformers," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 1998, pp. 132–133.
[104] D. Shaeffer and T. Lee, "A 1.5 V, 1.5 GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.
[105] M. Nakatsugawa, Y. Yamaguchi, and M. Muraguchi, "An L-band ultra low power consumption monolithic low noise amplifier," in *Tech. Dig. GaAs IC Symp.*, 1993, pp. 45–48.
[106] E. Heaney *et al.*, "Ultra low power low noise amplifiers for wireless communications," in *Tech. Dig. GaAs IC Symp.*, 1993, pp. 49–51.
[107] A. Schüppen, S. Gerlach, H. Dietrich, D. Wandrei, U. Seiler, and U. König, "1-W SiGe power HBT's for mobile communications," *IEEE Microwave Guided Wave Lett.*, vol. 6, pp. 341–343, Mar. 1996.
[108] P. A. Potyraj, K. J. Petrosky, K. D. Hobart, F. J. Kub, and P. E. Thompson, "A 230-watt S-band SiGe heterojunction junction bipolar transistor," *IEEE Trans. Microwave Theory Tech.*, vol. 44, pp. 2392–2397, Dec. 1996.
[109] D. R. Greenberg, M. Rivier, P. Girard, E. Bergeault, J. Moniz, D. Ahlgren, G. Freeman, S. Subbanna, S. J. Jeng, K. Stein, D. Nguyen-Ngoc, K. Schonenberg, J. Malinowski, D. Colavito, D. L. Harame, and B. Meyerson, "Large-signal performance of high-BVceo graded epi-base SiGe HBT's at wireless frequencies," in *Tech. Dig. Int. Electron Device Meeting*, 1997, pp. 799–802.
[110] E. O. Johnson, "Physical limitations on frequency and power parameters of transistors," *RCA Rev.*, pp. 163–177, 1965.
[111] K. Washio, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, and T. Onai, "A selective-epitaxial SiGe HBT with SMI electrodes featuring 9.3 ps ECL gate-delay," in *Tech. Dig. Int. Electron Device Meeting*, 1997, pp. 795–798.
[112] A. Schüppen, U. Erben, A. Gruhle, H. Kibbel, H. Schumacher, and U. König, "Enhanced SiGe heterojunction bipolar transistors with 160 GHz $f_{\max}$," in *Tech. Dig. Int. Electron Device Meeting*, 1995, pp. 743–746.
[113] L. Lanzerotti, J. Sturm, E. Stach, R. Hull, T. Buyuklimanli, and C. Magee, "Suppression of boron out-diffusion in SiGe HBT's by carbon incorporation," in *Tech. Dig. IEEE Int. Electron Device Meeting*, 1996, pp. 249–252.

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